

Semi-Conductor Laboratory

**SCL CAPABILITIES
AT A GLANCE**



VISION

- Create a strong research and development (R&D) base in the country in the field of microelectronics.
- Design & Development of devices in cutting-edge technology.
- Manufacture VLSI / MEMS-based systems & sub-systems .
- Transform SCL as a Centre of Excellence in Microelectronics in the country.





PREAMBLE

Semiconductor Laboratory (SCL), an autonomous body under the Ministry of Electronics and Information Technology (MeitY), Government of India, is the only Integrated Device Manufacturing Facility in the country providing end-to-end solutions for Development of Application Specific Integrated Circuits (ASICs), Opto-electronics devices, and Micro Electro Mechanical System (MEMS) Devices encompassing Design, Fabrication, Assembly, Packaging, Testing, and Reliability Assurance.

Formerly known as Semiconductor Complex Limited, a Government of India enterprise, it was converted into Semi-Conductor Laboratory under the Department of Space, Government of India, w.e.f. September 1, 2006. Administrative control of SCL, Society was transferred from the Department of Space (DoS) to the Ministry of Electronics and Information Technology (MeitY). SCL has an 8" wafer fab line qualified to the JEDEC-JP001A standard with a 180 nm CMOS technology node. SCL also has a 6" fab line for MEMS development and is expanding it to include a compound semiconductor fabrication facility. The VLSI design domain in SCL spreads over analog, digital, mixed-signal, memory, RF-CMOS, and optoelectronic in the form of silicon-proven and space-qualified ASICs, ASSPs, SoCs, SCL excels in developing ceramic packages and meets the demanding test requirements at the wafer & package level and reliability assurance adhere to global performance specifications such as MIL-PRF-38535 and MIL-STD-883. SCL possesses capabilities of the quality parameters of Ultra Pure Water (UPW) and bulk gases produced at SCL are at par with international standards. SCL brings decades of experience to provide customers with unparalleled microelectronics solutions in India. SCL is also engaged in the fabrication of Hi-Rel boards, Radio systems, and the indigenization of electronic subsystems.

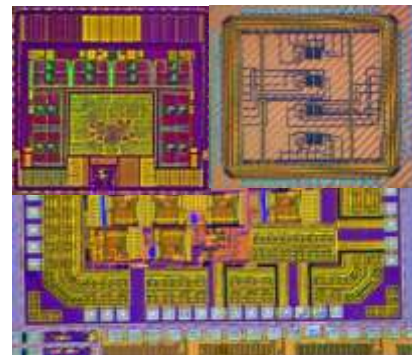


VLSI DESIGN

VLSI Design activity in SCL is spread over the domains of Analog, Mixed Signal, Digital, Power, Memory, RFCMOS, and Opto-Electronic. Various designs in the form of ASICs / ASSPs / SoCs/ Test Chips have been fabricated, tested, qualified, and delivered to end users. Besides, in-house design activities are pursued for the development and enhancement of products for potential future applications. Designs have been silicon-proven and qualified to space-grade or high reliability levels for induction in space and other strategic programs, as catalogued in the products section.

Key Design Domains

- Power Management
- Data Communication
- Data Converters
- Sensor Signal Conditioning
- Logic Design
- Memory
- RFCMOS
- Opto-Electronics - ROIC
- RadHard By Design
- SoC



Design Implementation Activities

- Feasibility Analysis
- Architecture Defining



- HDL Coding / Schematic Entry / Netlist Entry
- Electrical (Verification / Simulation)
- Synthesis
- DFT & ATPG
- Floorplan / Placement / CTS / Routing
- Full Custom Layout
- Physical Verification (DRC & LVS)
- Physical Parasitic Extraction (PEX)
- Physical STA / Post Layout Simulation
- Electro migration & IR drop analysis
- Chip Finishing & GDSII Release
- Design Automation

Memory Cuts & Cell Libraries

Type	Description
Standard Cells	1.8V- Standard Cell Library (540 cells; 10 Tracks)
Standard Cells (RHBD)	1.8V- Standard Cell Library (56 cells; 30 Tracks)
Memory Cuts	SP-SRAM : 4 metal 17 cuts, 6 metal 20 cuts ; DP-SRAM : 4 metal 20 cuts, 6 metal 20 cuts
I/O Cells	1.8V Core / 1.8V I/O ; 3.3V Core / 3.3V I/O ; 5.0V Core / 5.0V I/O ; 1.8V Core / 3.3V I/O ; 1.8V Core / 5.0V I/O



CMOS Process



SCL has standard 180nm CMOS baseline process technology. It enables the development of single-voltage or dual-voltage circuits requiring 1.8V, 1.8/3.3V, or 1.8V/5V power-supplies using its dual-gate oxide process, which features 4-6 Al-metal layers with thick-last metal. The process has add-on modules, namely 1.8V-HVt-transistors for low leakage, high-density precision MIM capacitors (1 or 1.7 or $2.8\text{fF}/\mu\text{m}^2$), high-

resistance poly (1 and $2\text{Kohms}/\text{sq.}$), Deep N-well for noise isolation, and more.

Baseline Process Technology Features

- 1.8V Core CMOS.
- 1.8V or 3.3V I/O.
- Single poly & upto 6 Metal Layers with USG-BEOL.
- 23-34 Mask layers (depending on Metal Layers and Analog modules).

Analog Process Modules

- High-Vt (Low leakage current ~one order less).
- Metal Insulator Metal capacitor: Single MIM (1 & $2\text{fF}/\mu\text{m}^2$) & stacked MIMs ($2\times$).
- Deep N-Well (Isolated p-wells for substrate noise isolation).
- High resistance poly silicon resistor: HIPO ($1\text{k}\Omega/\text{sq}$; $2\text{k}\Omega/\text{sq}$).
- Thick Last metal ($2\mu\text{m}$).
- 5V-MOSFETs (Gox: 110A).



MEMS Fabrication Facility

SCL has state-of-the-art 6" fab line for MEMS based devices and detector development and is expanding it to include a compound semiconductor fabrication facility for the production of optoelectronic and high-power devices.



The key features are:

- 6" Process Equipment Line, In-line Inspection & Metrology Tools and Support Utilities as per international standards.
- Clean Rooms of Class 10 & Class 100 (Post CMOS) with controlled environmental conditions.
- Dedicated bays for Wafer Fabrication Processes viz. Diffusion (High temperature furnaces), Lithography (5X stepper, 1X aligner, coater developer track), Etching (Dry & Wet), Implantation (High and medium current implanters), Thin Films (PVD & CVD furnaces for dielectrics and metals) working seamlessly from Wafer-in to Wafer-out.
- MEMS Specific fabrication capabilities like wafer bonding, electroplating, glass wafer processing, Vapor HF, CPD etc.
- Characterization facility including Laser Doppler Vibrometer, Nanoindenter, AFM, XRD, 4 Point Probe resistance measurement.



VLSI ASSEMBLY & PACKAGING

VLSI and MEMS Packaging facility operating in Class 100 and Class 10000 Clean Rooms includes Die Bonders, Ball and Wedge Wire Bonders, Multi-Zone Furnaces for Hermetic Sealing, Multi Function Bond Pull Testers, Laser Welder, Dicing Saw, Tape Mounter etc.



Key capabilities

- Package design lab catering the bonding and device drawing generations for all devices for post Fab activities.
- Design and analysis of Single die and multi-die substrates (SiP) to optimise the Signal and Power Integrity performances for CMOS, Imager & RF devices.
- Design, analysis and development for MEMS packaging
- Thermo - mechanical design, analysis & characterisation for devices
- Layout of IC package and generation of fabrication inputs for developing custom package.
- Standard IC packages and Custom Substrate development end to end solutions.
- Fine Pitch Bonding capability (using 0.8, 1 & 1.25mil wire) for pad size of $57\mu\text{m} \times 57\mu\text{m}$ and 65 μm pitch
- Low Temperature Process for packaging large dies of Imager devices
- Multi-Chip Packaging Process for ASICs and sensor devices



VLSI TEST FACILITY

VLSI and MEMS Test Facilities meet the demanding test requirements of complex, high-speed, and high-pin count Integrated Circuits in the digital, mixed-signal, and Analog domains. The Facility also caters to the testing of a variety of MEMS and RF devices, such as Pressure, Temperature & Humidity Sensors, Accelerometers, RF switches, and Band-Pass Filters.



Test plans and engineering activities implemented at various stages of product development include:

- Prototype Testing/Debug at wafer and device level
- Post Silicon Validation and characterization
- Production testing on Automatic Test Equipment

Key capabilities

- Class 10000 clean room with 8" and 6" Automatic Wafer Prober, VLSI Testers, Temperature characterization setup, MEMS device test setups including Shaker, Laser Doppler Vibrometer (LDV), Thermal Chamber, Pressure calibrator etc.
- Capability to build semi-automatic test setups for electrical design validation and characterisation of CMOS and MEMS devices. Various such test setups for CMOS ASICs, CCD detectors and Low Drop Out Regulators, Process Evaluation



Vehicles like Ring Oscillators and Band Gap Reference Circuits have been developed in-house.

- In-house development capability to develop blade-type probe cards up to 120-pin up to 90 μ m pad pitch. We have design capability of developing high-pin count epoxy probecards with pitch up to 65 μ m exceeding 400 pads.
- Characterization of Digital, Mixed Signal and Analog devices from -55°C to 125°C up to 512 I/O's (800 MHz clock rate) Expertise to develop Test Programs for variety of devices such as amp etc.
- Design capability for multilayer & high speed Device Interface Boards and Prober Interface Boards
- Characterization of Pressure Sensors (up to 600 bar), Temperature Sensors (-90°C to 180°C), Humidity Sensors (10% RH to 95% RH) & Accelerometers (up to 20g)
- Programming languages like C, C#, Visual Basic, MATLAB, LabView etc. have been used to develop test programs on various testers to test digital, analog and mixed-signal CMOS devices.



RF TEST FACILITIES

SCL has in-house testing capability for RF circuits for both wafer level and package level up to 40 GHz. Full RF and DC characterizations can be carried out in-house. The capabilities of major equipment are mentioned below:

- Vector Network Analyzer VNA):
- Spectrum Analyzer: Up to 26.5GHz with Noise Figure measurement
- Signal Generator: 250 KHz to 40GHz , +4dBm to -130dBm, Modulation-Amplitude Frequency & Phase
- Impedance Analyzer: 1 MHz to 3 GHz, Measurements $|Z|$, $|Y|$, L_s , L_p , C_s , C_p , R_s , R_p , X , G , B , D , Q , Γ , z , ϵ_r , μ_r , $\tan \delta$
- Power Meter: DC-40 GHz, -30 dBm to +20 dBm
- RF Prober: Manual (Summit 11K) and Semi-Automatic (Summit12K) RF Prober with thermal control chuck





MEMS TEST FACILITIES

SCL has in-house testing capability for MEMS circuits. The capabilities of major equipment are mentioned below:

Temperature Calibrator:-

Temperature Range:-

-35°C to 100°C (Ethanol)

35°C to 280°C (Silicon Oil)

Reference High Precision PRT

Temperature Range: -200 °C to 661 °C

Basic Accuracy: ± 0.006 at 0°C

- VibShaker:-Max. Acceleration: 110g; Frequency range: 7KHz
- Laser Doppler Vibrometer
- Wafer Prober
- Pressure Controller / Calibrator:-
 - Upto 200 Bar (Automatic Calibrators):
 - 1.6 Bar
 - 1.6 bar, 20 Bar
 - 50 Bar
 - 70 mBar, 200 Bar upto 600 Bar (Manual, Dead Weight Calibrator)
- Vacuum Pumps
- Temperature Chambers
- Temperature Range: -70°C to 180°C ; Accuracy: $\pm 0.5^\circ\text{C}$





RELIABILITY & QUALITY ASSURANCE

The Reliability & Quality Assurance of the devices / boards / sub-systems / systems manufactured at SCL is maintained throughout design, chip fabrication, assembly / packaging and testing phases. Regular inline QA inspection / audits are carried out to ensure defect



free manufacturing. Screening and qualification of products for required applications is an integral part of the process. The reliability and quality assurance requirements are guided by global performance specifications as per MIL-PRF-38534, MIL-PRF-38535, JEDEC, MIL-883 and other relevant standards. Continuous improvements in processes are implemented through feedbacks at appropriate stages and performing failure analysis.

Facility for Environmental Test

- Process Reliability Test System.
- Thermal Shock Chamber (Air to Air).
- Thermal Shock Chamber (Liquid-to-Liquid).
- Vibration Test System.
- High Temperature, High Humidity Chamber.
- Fine & Gross Leak Test Systems for Hermeticity Check.
- Life Operating Test Systems (Burn-In Chambers).



- Constant Acceleration Test System.
- Mechanical Shock Tester.
- Particle Impact Noise Detection (PIND) Tester.
- Electro Static Discharge (ESD) Simulator based on Human Body Model (HBM).

Facility for Environmental Test

- Scanning Electron Microscope (SEM).
- Focused Ion Beam System (FIB).
- Energy Dispersive X-Ray Spectrometer (EDX).
- Micro Cleaver.
- Polisher Grinder.
- Optical Microscopes.

Key Capabilities

- Screening & Qualification of VLSI devices / ASICs / MEMS devices / boards / sub-systems / systems.
- Process Qualification.
- Device Failure Analysis.
- Process Audits.
- Quality System & Documentation Control.



ELECTRO-OPTICS/DETECTOR TECHNOLOGY

SCL has a long established fabrication process for Silicon Charge Coupled Device (CCD) based image sensors in the visible range (400nm to 1000nm) for remote sensing for cartography and resource mapping applications.

These detectors are also to be used for satellite attitude and orbital control in the form of star sensors.

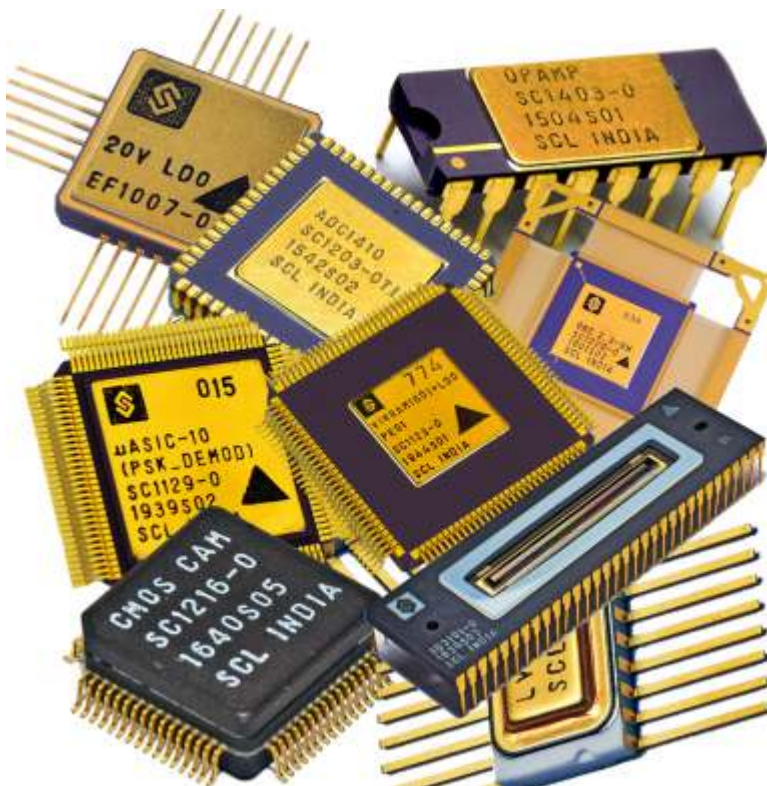
Facility is in place for bare detectors, assembly, testing and flight qualification of Detectors.

Key Detectors developed include

- Photodiode detector based CCD linear imager with 4K elements for Indian Mini Satellite (IMS-1).
- Further 1K x 1K Frame Transfer CCD image sensor for star sensor applications and is flight qualified for space use.
- Hyperspectral image sensor fabricated in SCL with a 1000 (spatial) x 66 (spectral) for HySIS satellite.
- 4000 element x 48 stage Frame Transfer CCD sensors in Thirteen different bands for the Ocean Colour Monitor (OCM-3) payload of Oceansat-3 is under qualification.
- SCL has also worked in collaboration with other strategic organizations to develop Silicon Photomultiplier (SiPM) and large area diode sensors for various scientific and other applications.
- Current efforts to further enhance the existing technology by introducing anti-blooming capabilities, enhancing short wavelength response and increasing radiation hardness which will allow the use of detectors developed in SCL, in more demanding applications.



**SCL
PRODUCTS**

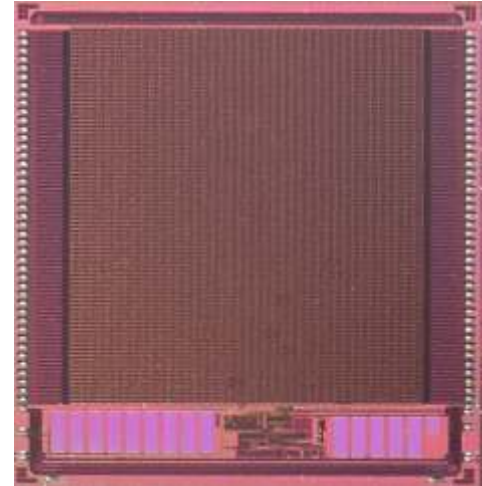




LOW DROP-OUT LINEAR VOLTAGE REGULATOR 1.2V, 1.6A

PRODUCT DESCRIPTION:

This LVR supplies a nominal voltage of 1.2V to a circuit or load. The output voltage of the voltage regulator is regulated by the internal circuitry of the regulator to be relatively independent of the current drawn by the load, the supply or line voltage, and the ambient temperature. It is stable with an external capacitor not lower than 10uF of ESR 1ohm to 10ohm. In order to protect voltage regulator from excessive temperatures or accidental short circuit, Over-temperature shutdown and programmable Over-current shutdown circuit are included in this chip.

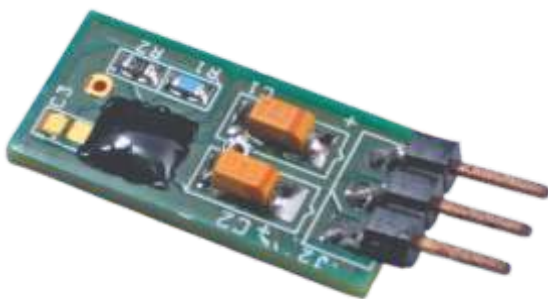


FEATURES:

- Nominal V_{OUT} : 1.2V
- Maximum output current: 1.6A
- Dropout Voltage at full load < 400mV
- Line regulation: < 2%/V; Load regulation: < 1%
- Quiescent current (I_{GND}): 14mA
- Max Supply V_{IN} : 3.6V
- Power Good Flag: -5% of V_{NOM}
- Over temperature shutdown with Disable Feature
- Programmable Short Circuit Current Shutdown after 1 sec delay
- Operating Temperature (T_A): -55°C to +125°C
- SCL's 180nm CMOS Technology
- Dies/Customized Package Options



LOW DROP-OUT LINEAR VOLTAGE REGULATOR 1.8V, 150mA



PRODUCT DESCRIPTION:

This LVR provides a fixed output voltage of 1.8V, 150mA full load current. It is stable with an external capacitor not lower than 4.7uF of ESR 1 ohm to 10 ohm. It supplies a nominal voltage of 1.8V to a circuit or load. The output voltage of the voltage regulator is regulated by the internal circuitry of the regulator to be relatively independent of the current drawn by the load, the supply or line voltage, and the ambient temperature. In order to protect voltage regulator from excessive temperatures or accidental short circuit, Over-temperature and Over-current protection circuit are included in this chip. Power good pin indicates whether output is within range of $\pm 10\%$ of nominal output.

FEATURES:

- Nominal V_{OUT} : 1.8V
- Maximum output current: 150mA
- Dropout Voltage at full load: < 400mV
- Quiescent current (IGND): 9mA
- Voltage accuracy line and load: <0.5%
- Power Good feature: $\pm 10\%$ of V_{NOM}
- Max Supply VIN: 3.6V
- Over temperature shutdown with Disable Feature
- Short circuit current limiting feature: 350mA
- Operating Temperature (TA): -55°C to +125°C
- SCL's 180nm CMOS Technology
- Dies/Customized Package Options



LOW DROP-OUT LINEAR VOLTAGE REGULATOR 1.8V, 800mA

PRODUCT DESCRIPTION:

This LVR provides a fixed output voltage of 1.8V, 800mA full load current. It is stable with an external capacitor not lower than 10uF of ESR 1 ohm to 10 ohm. It supplies a nominal voltage of 1.8V to a circuit or load. The output voltage of the voltage regulator is regulated by the internal circuitry of the regulator to be relatively independent of the current drawn by the load, the supply or line voltage, and the ambient temperature. In order to protect voltage regulator from excessive temperatures or accidental short circuit, Over-temperature and Over-current protection circuit are included in this chip. Power good pin indicates whether output is within range of -5% and +10% of nominal output.



FEATURES:

- Nominal V_{OUT} : 1.8V
- Maximum output current: 800mA
- Dropout Voltage at full load: < 200mV
- Quiescent current (I_{GND}): 10mA
- Voltage accuracy line and load: <1%
- Power Good feature: -5% and +10% of V_{NOM}
- Max Supply V_{IN} : 3.6V
- Over temperature shut down with Disable Feature
- Programmable Short circuit current limiting feature
- Operating Temperature (T_A): -55°C to +125°C
- SCL's 180nm CMOS Technology
- Dies/Customized Package Options



LOW DROP-OUT LINEAR VOLTAGE REGULATOR 1.8V, 1.6A



PRODUCT DESCRIPTION:

This LVR supplies a nominal voltage of 1.8V to a circuit or load. The output voltage of the voltage regulator is regulated by the internal circuitry of the regulator to be relatively independent of the current drawn by the load, the supply or line voltage, and the ambient temperature. In order to protect voltage regulator from excessive temperatures or accidental short circuit, Over-temperature shutdown and programmable Over-current shutdown circuit are included in this chip. It is stable with an external capacitor not lower than 10uF of ESR 1ohm to 10ohm.

FEATURES:

- Nominal V_{OUT} : 1.8V
- Maximum output current: 1.6A
- Dropout Voltage at full load < 300mV
- Line regulation: < 2%
- Load regulation: < 1%
- Quiescent current (I_{GND}): 14mA
- Max Supply V_{IN} : 3.6V
- Power Good: -5% of V_{NOM}
- Over temperature shutdown with Disable Feature
- Programmable Short Circuit Current Shutdown after 1sec delay
- Operating Temperature (T_A): -55°C to +125°C
- SCL's 180nm CMOS Technology
- Dies/Customized Package Options



LOW DROP-OUT LINEAR VOLTAGE REGULATOR 3.3V, 200mA

PRODUCT DESCRIPTION:

The 3.3 V output, 200mA full load current LVR provides a fixed output voltage of 3.3 V for a wide range of input operating voltage from 3.7 V to 6 V. The LVR is stable with an external capacitor not lower than 4.7uF of ESR 0.1 ohm to 10 ohm. SC1019-0 is mainly intended for integration with digital, analog and RF chips.

In order to protect voltage regulator from excessive temperatures or accidental short circuit, Over-temperature protection circuit and short circuit fold-back current limiting feature are included in this chip. Device will go in to Short circuit fold-back at twice of FL, i.e., 0.4A.

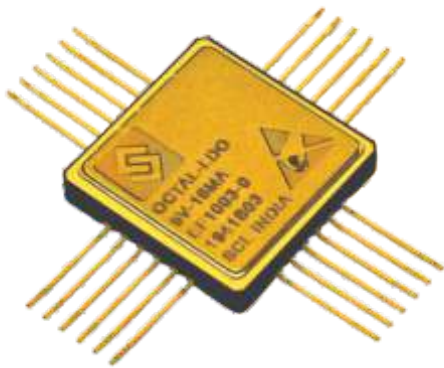


FEATURES:

- Nominal $V_{OUT} = 3.3V$
- Full load current = 200mA
- Low quiescent current of <1 mA
- Dropout Voltage at full load < 150mV
- Max Supply V_{IN} : 6V
- Over temperature shut down mechanism
- Short circuit fold-back current limiting feature: 400mA
- Operating Temperature (T_A): -55°C to +125°C
- SCL's 180nm CMOS Technology
- Packaged in COB package
- Dies/Customized Package Options



OCTAL-CORE LOW DROP-OUT LINEAR VOLTAGE REGULATOR 5V, 16mA



PRODUCT DESCRIPTION:

The LVR has independent supplies a nominal voltage of 5V to a circuit or load, and it can deliver up to 16 mA per channel of output current. Internally, this linear regulator consists of a reference, an error amplifier, and a P-channel MOSFET pass transistor. It has 8 independent cores.

FEATURES:

- Nominal output voltage: 5V
- Eight Independent Cores
- Maximum output current per core: 16mA
- Dropout voltage: 500mV
- Voltage accuracy over line & load: 1%
- Fold back current at 19mA
- Fold back recovery at 5mA
- Max Supply V_{IN} : 7.5V
- Operating Temperature (T_A): -55°C to +125°C
- 24 Pin CFP/ Customized Package Options /Die



PROGRAMMABLE BIAS GENERATOR, 0.5V-2.1V, 8-Bits, 5mA

PRODUCT DESCRIPTION:

It is 8-bit programmable dual channel output bias voltage generator with dynamic range of 1.6V (0.5V to 2.1V). It has band-gap reference block, voltage reference block, two R-2R DACs; two band limited operational amplifier. It has a four wire serial interface. The digital input byte is converted to corresponding analog output with help of DAC (Digital to Analog Converter).

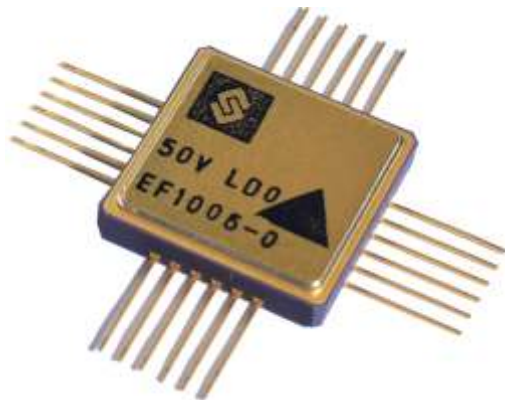


FEATURES:

- Line voltage: 3.0V-3.6V
- Dynamic range: 1.6V (0.5V to 2.1V)
- Resolution: 8bits
- Output drive current per channel: 5mA
- Two Programmable outputs
- Output enable/disable feature
- Programming Interface: 4wire serial
- Clock input: LVCMOS compatible
- Low Power Dissipation
- Operating Temperature (T_A): -55°C to +125°C
- SCL's 180nm CMOS Technology
- Packaged in 20 Lead Side Brazed package
- FM Qualified as per MIL STD 883



HIGH VOLTAGE, QUAD SOLID STATE SWITCH 27V-42V, 1.0A



PRODUCT DESCRIPTION:

It has four independent switches in a single die. It can switch 1A load at 42V. This switch transistor is controlled through a control circuit. The control circuit operates from input voltage. When the control input is high (5V), the switch conducts and provides the load current (1A). Otherwise this switch remains off. The input voltage may be as low as 3.5V to be considered as High (>3.5V) which can turn on transistor.

FEATURES:

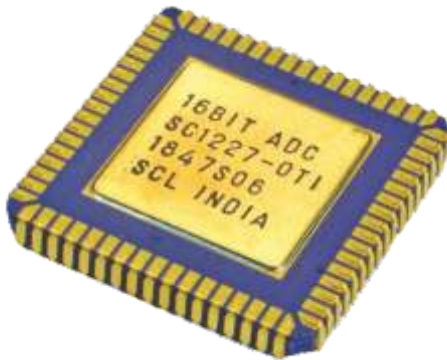
- Raw bus voltage: 27V-42V
- Full load current: 1A
- Control voltage: 3.5V to 5.5V
- Output drop (VSD): < 650mV at 1A
- Input (leakage) current: 0.19mA
- Quiescent current (IGND): 40nA
- Operating Temperature (T_A): -55°C to +125°C
- Packaged in 48 Pin CFP



DATA CONVERTERS (ADC & DAC)



16-BIT, 5 MSPS, PIPELINE ANALOG TO DIGITAL CONVERTER WITH ON CHIP VOLTAGE REFERENCE



PRODUCT DESCRIPTION:

The 16-bit, 5-MSPS is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 16-bit digital word at 5 Mega samples per second (MSPS) and designed for imaging applications. This converter uses a differential, pipeline architecture with digital error correction. Operating on a single 3.3V power supply, device achieves ≥ 13 -bits effective resolution at Nyquist rate and consumes $<130\text{mW}$. The Power Down feature reduces power consumption to $<15\text{mW}$. The differential inputs provide a full scale differential input swing equal to 4 times of VREF ($4 \times (\text{CAPTE} - \text{CAPBE})$). Full scale input range is recommended for optimum performance.

FEATURES:

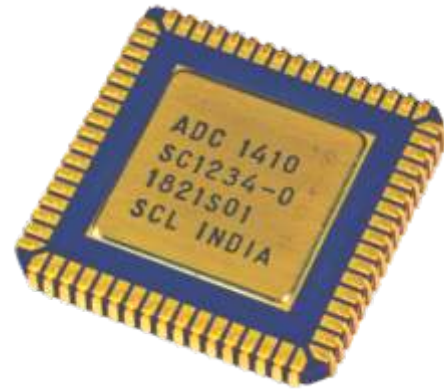
- Operating Voltage: $3.3\text{V} \pm 0.3\text{V}$
- Resolution: 16-Bit
- Data Rate: 5MSPS
- Input Range : 2Vp-p Diff. /Single Ended
- On-Chip Voltage References
- No missing code Guaranteed
- Output Data Format: Straight Binary
- Data Latency: 7 Clock Cycles
- Power Consumption $<130\text{mW}$
- Power Down Mode
- Operating Temperature (T_A): -55°C to $+125^\circ\text{C}$
- SCL's 180nm CMOS Technology
- Package: 68 PIN CQFP-J
- θ_{jc} : 4.81°C/W



14-BIT, 10MSPS, PIPELINE ANALOG TO DIGITAL CONVERTER WITH ON CHIP VOLTAGE REFERENCE

PRODUCT DESCRIPTION:

The 14-bit 10-MSPS is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 14-bit digital word at 10 Mega samples per second (MSPS) and designed for imaging applications. This converter uses a differential, pipeline architecture with digital error correction. Operating on a single 3.3V power supply, device achieves > 12-bits effective resolution at nyquist rate and consumes <250mW power. The Power Down feature reduces power consumption to <50mW. The differential inputs provide a full scale differential input swing equal to 4 times of VREF ($4 \times (CAPTE - CAPBE)$). Full scale input range is recommended for optimum performance. The ASIC is fabricated in 0.18 μ m SCL CMOS Standard Logic Process.



FEATURES:

- Operating Voltage: 3.3V
- Resolution: 14-Bit
- Data Rate: 10MSPS
- Input Range : 2Vp-p Differential / Single Ended
- On Chip Voltage References
- No missing code Guaranteed
- Output Data Format: Straight Binary
- Data Latency: 8 Clock Cycles
- Power Consumption < 250mW
- Power Down Mode
- SCL's 180nm CMOS Technology
- Operating Temperature (T_A): -55°C to +125°C
- Package: 68 PIN CQFP-J
- θ_{jc} : 4.81° C/W



14-BIT, 5MSPS, LOW POWER PIPELINE ANALOG TO DIGITAL CONVERTER



PRODUCT DESCRIPTION:

The 14-bit 5 MSPS is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 14-bit digital word at 5 Mega samples per second (MSPS) and designed for imaging applications. This converter uses a differential, pipeline architecture with digital error correction. Operating on a single +3.3V power supply, device achieves >12.0 bits effective resolution at nyquist rate and consumes <100mW. The Power Down feature reduces power consumption to 50mW. The differential inputs provide a full scale differential input swing equal to 4 times of VREF (=CAPTE-CAPBE). Full scale input range is recommended for optimum performance. The chip requires three external references as 1.9V, 1.65V and 1.4V. The device has on chip voltage reference. To use internal reference, external buffer must be provided between internal and external references.

FEATURES:

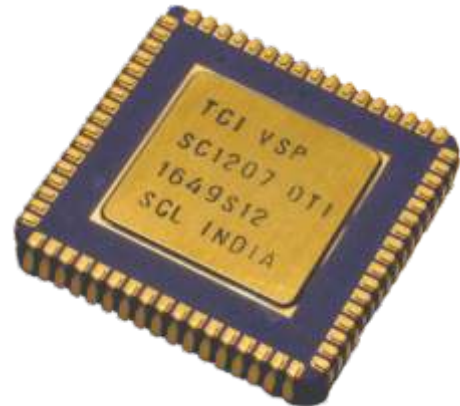
- Operating Voltage: 3.3V
- Resolution: 14-Bit
- Data Rate: 5MSPS
- 2Vp-p Differential/Single Ended Input
- No Missing Code guaranteed
- Data Latency 8 Clock Cycles
- Output straight Binary Format
- Power Consumption <100mW
- Power Down Mod
- SCL's 180nm CMOS Technology
- Operating Temperature (T_A): -55°C to +125°C
- 68 PIN CQFP-J Package
- θ_{jc} : 4.81° C/W



12-BIT, 8MSPS LOW POWER PIPELINE ANALOG TO DIGITAL CONVERTER

PRODUCT DESCRIPTION:

The 12-bit 8 MSPS is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 12-bit digital word at 8 Mega samples per second (MSPS) and designed for imaging applications. This converter uses a differential, pipeline architecture with digital error correction. The Power Down feature reduces power consumption to 50mW. The differential inputs provide a full scale differential input swing equal to 4 times of $V_{REF} (= CAPTE - CAPBE)$. Full scale input range is recommended for optimum performance. The chip requires three external references as 1.9V, 1.65V and 1.4V. The device has on chip voltage reference. To use internal reference, external buffer must be provided between internal and external references. The chip requires three external references as 1.9V, 1.65V and 1.4V. The device has on chip voltage reference. To use internal reference, external buffer must be provided between internal and external references

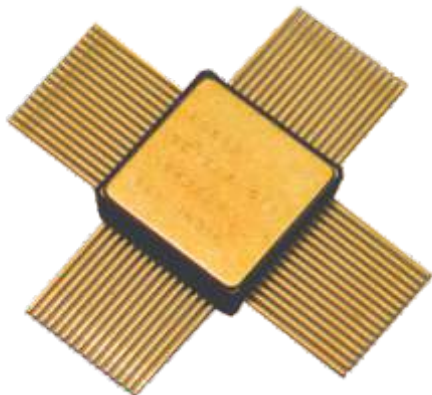


FEATURES:

- Operating Voltage: 3.3V
- Resolution: 12-Bit
- Data Rate: 8MSPS
- 2Vp-p Differential/Single Ended Input
- No Missing Code guaranteed
- Output straight Binary Format
- Data Latency 8 Clock Cycles
- Power Consumption <110mW
- Power down Mode
- SCL's 180nm CMOS Technology
- Operating Temperature (T^A): -55°C to +125°C
- 68 PIN CQFP-J Package
- θ_{jc} : 4.81° C/W



8-BIT, 50MSPS, LOW POWER, PIPELINE ANALOG TO DIGITAL CONVERTER



PRODUCT DESCRIPTION:

The 8-bit 50MSPS is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 8-bit digital word at 50 Mega samples per second (MSPS) and designed for imaging and communication applications. The converter uses a differential, pipeline architecture with digital error correction. Operating on a single 3.3V power supply, device achieves 8-bits effective resolution at nyquist rate and consumes <420mW power. The Power Down feature reduces power consumption to <15mW. The differential inputs provide a full scale differential input swing equal to 4 times of VREF ($4 \times (CAPTE - CAPBE)$). Full scale input range is recommended for optimum performance. The chip requires three external references as 1.9V, 1.65V and 1.4V. The device has on chip voltage reference. To use internal reference, external buffer must be provided between internal and external references

FEATURES:

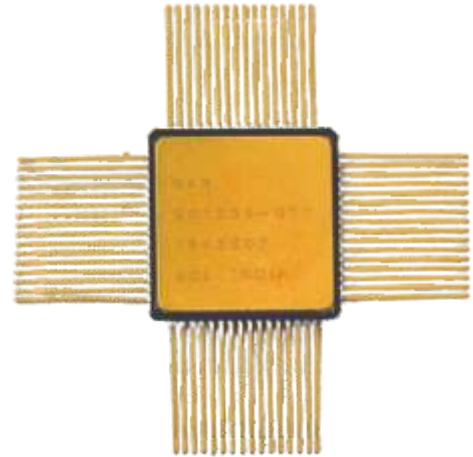
- Operating Voltage: 3.3V
- Resolution: 8-Bit
- Data Rate: 50MSPS
- 2Vp-p Differential/Single Ended Input
- On Chip Voltage References
- No Missing Code guaranteed
- Output straight Binary Format
- Data Latency 4 Clock Cycles
- Power Consumption < 420mW
- Power Down Mode
- SCL's 180nm CMOS Technology
- Operating Temperature (T_A): -55°C to +125°C
- 64 PIN CQFP Package
- θ_{jc} : 4.03° C/W



8-BIT, 1MSPS SUCCESSIVE APPROXIMATION ANALOG TO DIGITAL CONVERTER

PRODUCT DESCRIPTION:

The 8-bit SAR is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 8-bit digital word at 1 Mega samples per second (MSPS) and designed for imaging applications. This converter uses a SAR architecture, operating on a single 3.3V power supply, device achieves 8-bits effective resolution at nyquist rate and consumes <10mW power. The inputs provide a full scale input swing equal to 3.3V. Full scale input range is recommended for optimum performance. The ASIC is fabricated in 0.18μm SCL CMOS Standard Logic Process.



FEATURES:

- Operating Voltage: 3.3V
- Resolution: 8-Bit
- Data Rate: 1MSPS
- Input Range: 3.3Vp-p Single Ended
- No missing code Guaranteed
- Output Data Format: Straight Binary
- Power Consumption < 10mW
- SCL's 180nm CMOS Technology
- Operating Temperature (T^A): -55°C to +125°C
- Packaged in 64 Pins, CQFP
- θ_{jc} : 4.03° C/W



12-BIT,1MSPS, 4-CORE SUCCESSIVE-APPROXIMATION -REGSITER(SAR) ANALOG TO DIGITAL CONVERTER



PRODUCT DESCRIPTION:

The 8-bit SAR is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 8-bit digital word at 1 Mega samples per second (MSPS) and designed for imaging applications. This converter uses a SAR architecture, operating on a single 3.3V power supply, device achieves 8-bits effective resolution at nyquist rate and consumes <10mW power. The inputs provide a full scale input swing equal to 3.3V. Full scale input range is recommended for optimum performance. The ASIC is fabricated in 0.18 μ m SCL CMOS Standard Logic Process.

FEATURES:

- Operating Voltage: 3.3V
- Resolution: 8-Bit
- Data Rate: 1MSPS
- Input Range: 3.3Vp-p Single Ended
- No missing code Guaranteed
- Output Data Format: Straight Binary
- Power Consumption < 10mW
- SCL's 180nm CMOS Technology
- Operating Temperature (TA): -55°C to +125°C
- Packaged in 64 Pins, CQFP
- θ_{jc} : 4.03° C/W



14-BIT, 10MSPS CCD ANALOG SIGNAL PROCESSOR WITH ON CHIP VOLTAGE REFERENCE

PRODUCT DESCRIPTION:

This is fully integrated, high performance analog signal processor for CCD applications. It features a single channel architecture designed to sample and conditions the outputs of CCD arrays. Signal paths utilize Correlated Double Sampler (CDS), 6-bit Programmable Gain Amplifiers (PGA), and 9-bit offset correction DAC for black level correction of input. The PGA and offset DAC are programmed independently allowing unique values of gain and offset for inputs. The internal registers can be programmed through a 4-wire serial digital interface. A programmable feature includes gain adjustment, black level correction, programmable delay and input bandwidth control. This converter uses a differential, pipeline architecture with digital error correction. The Power Down feature reduces power consumption to 25mW. The differential inputs provide a full scale differential input swing equal to 2 times of VREF (=CAPTE-CAPBE).



FEATURES:

- Operating Voltage: 3.3V
- Resolution: 14Bits
- Data Rate: 10MSPS
- 1Vp-p Differential /Single Ended Input
- On Chip Voltage References
- No Missing Code Guaranteed
- Output straight Binary Format
- Data Latency 9 Clock Cycles
- Power Consumption < 250mW
- Power Down Mode
- 64 PGA Gain Steps 1 to 6 PGA Gain Ranges
- 9Bit Offset Correction
- $\pm 60\text{mV}$ Offset Correction
- SCL's 180nm CMOS Technology
- 100 PIN CQFP Package
- θ_{jc} : 0.99° C/W



SINGLE CHANNEL, 12-BIT, 5MSPS CCD ANALOG SIGNAL PROCESSOR



PRODUCT DESCRIPTION:

This is fully integrated, high performance analog signal processor for CCD applications. It features a single channel architecture designed to sample and conditions the outputs of CCD arrays. Signal paths utilize Correlated Double Sampler (CDS), 6-bit Programmable Gain Amplifiers (PGA), and 9-bit offset correction DAC for black level correction of input. The PGA and offset DAC are programmed independently allowing unique values of gain and offset for inputs. The internal registers can be programmed through a 4-wire serial digital interface. A programmable feature includes gain adjustment, black level correction, programmable delay and input bandwidth control. This converter uses a differential, pipeline architecture with digital error correction. The Power Down feature reduces power consumption to 25mW. The differential inputs provide a full scale differential input swing equal to 2 times of VREF (=CAPTE-CAPBE). The chip requires three external references as 1.9V, 1.65V and 1.4V. The device has on chip voltage reference. To use internal reference, external buffer must be provided between internal and external references.

FEATURES:

- Operating Voltage: 3.3V
- Resolution: 12Bits
- Data Rate: 5MSPS
- 1Vp-p Differential /Single Ended Input
- On Chip Voltage References
- No Missing Code Guaranteed
- Output straight Binary Format
- Data Latency 9 Clock Cycles
- Power Consumption < 170mW
- Power Down Mode
- 64 PGA Gain Steps 1 to 6 PGA Gain Ranges
- 9Bit Offset Correction DAC Resolution
- $\pm 60\text{mV}$ Offset Correction DAC Range
- SCL's 180nm CMOS Technology
- 100 PIN CQFP Package
- θ_{jc} : 0.99° C/W



12 BIT, 20MSPS DIGITAL TO ANALOG CONVERTER

PRODUCT DESCRIPTION:

The SC1605 is a two channel (complementary output) precision fully integrated 12 bit digital to analog converter with full scale current of 2mA. It has got an on chip precise low drift voltage reference of 1.2V. There is an option of disabling the on chip reference to apply external reference. Latches are provided for high speed synchronization providing better AC characteristics for DAC. Additional option is provided for disabling the latches in case latches have to be bypassed. On chip power on reset is also provided so that the chip output doesn't go to unknown state at the time of power on.



FEATURES:

- Operating Voltage: 3.3V
- Resolution: 12 Bits
- Data Rate: 20MSPS
- 2mA Full Scale Input Range
- Power Down Mode
- Monotonicity Guaranteed
- Power On Reset
- On Chip 1.2V Reference
- Power Down Feature
- SCL's 180nm CMOS Technology
- 64 Pin CERQUAD Package
- θ_{jc} : 3.77° C/W



4 CHANNELS, 24-BIT Σ - Δ ANALOG TO DIGITAL CONVERTER (RADIATION HARDENED)



PRODUCT DESCRIPTION:

The SC1218-0 is a precision, wide range, Sigma-Delta, Analog-to-Digital converter with 24-bit resolution operating from 3.0V to 3.6V. It has fully four differential multiplexed channels. The PGA (Programmable Gain Amplifier) provides selectable gains of 1 to 128 in binary steps with an effective resolution of 19 bits at PGA 1 and OSR of 2048. It uses a second order Sigma Delta Modulator that converts the analog input signal in to a digital pulse train whose average duty cycle represents the digitized signal information. The pulse train is then processed by a digital sinc3 filter to produce a digital output. The decimation ratio of the digital filter can be programmed by user either to achieve higher accuracy or higher throughput. SC1218-0 has digitally on-chip offset and gain calibration. The serial interface is SPI Compatible. It can be configured to scan all the signal input sequentially with minimum communication overhead.

FEATURES:

- 24 BITS NO MISSING CODES1
- 0.003% INL
- 19 BITS EFFECTIVE RESOLUTION (PGA = 1, OSR=2048)
- 12 BITS (PGA = 128, OSR=2048)
- PGA FROM 1 TO 128 (BINARY STEPS)
- PROGRAMMABLE DATA OUTPUT RATES UP TO 20KSPS
- PRECISION ON-CHIP 1.22V REFERENCE ACCURACY : 1.5%
- DRIFT: ± 20 ppm of REFOUT
- EXTERNAL DIFFERENTIAL REFERENCE Upto 2.5V
- ON-CHIP CALIBRATION
- SPI COMPATIBLE
- 3.0V TO 3.6V
- RAD HARDENED (TID) UPTO 300KRAD
- SEL/SEU IMMUNE UPTO 50 LET MEV-cm²/mg
- 180nm SCL CMOS STANDARD LOGIC PROCESS
- ESD PROTECTION UPTO ± 3 KV HBM
- $\Theta_{jc} = 3.7^{\circ}\text{C/W}$



4 CHANNELS, 24-BIT Σ - Δ ADC WITH INPUT OFFSET DAC (RDAS)

PRODUCT DESCRIPTION:

The RDAS is a precision, wide range, Sigma-Delta, Analog-to-Digital converter with 24-bit resolution operating from 2.97 V to 3.6V for sensor signal conditioning application. It has fully four differential multiplexed channels. The PGA (Programmable Gain Amplifier) provides selectable gains of 1 to 128 in binary steps with an effective resolution of 19 bits at PGA 1 and OSR of 2048. It uses a second order Sigma Delta Modulator that converts the analog input signal in to a digital pulse train whose average duty cycle represents the digitized signal information. The pulse train is then processed by a digital sinc3 filter to produce a digital output. The decimation ratio of the digital filter can be programmed by user either to achieve higher accuracy or higher throughput. SC1213-0 has digitally on-chip offset and gain calibration. It also contains 8 Bits Input offset DAC for adjusting the offset and two 8-bits current DAC with three different ranges. The serial interface is SPI Compatible.



FEATURES:

- 4 Multiplexed Differential Input Channel
- 24 Bits Σ - Δ ADC
- No missing code
- PGA from 1 to 128 (Binary Steps)
- 8-Bit Input Offset DAC at each PGA
- Two 8 Bits IDAC (three different range)
- INL : 0.020%
- 19 Bits ENOB (PGA = 1, OSR=2048)
- 12 Bits ENOB (PGA = 128, OSR=2048)
- Programmable Data Rate upto 5KSPS
- Precision on-chip 1.22V Reference Accuracy: 1.0%, Drift: ± 40 ppm
- On-chip Calibrations
- SPI Compatible
- 2.97V TO 3.6V
- POWER CONSUMPTION < 10mW



16 CHANNELS SIMULTANEOUS SAMPLING 24 BIT Σ - Δ ADC (MULTI-CORE RDAS1.1)

PRODUCT DESCRIPTION:

Multi-Core Reconfigurable Data Acquisition System (Multi-Core RDAS) is a fully integrated data acquisition system. It incorporates 16 high resolution Sigma Delta ($\Sigma\Delta$) ADCs, 32 Eight Bits IDACs along with the calibration and over-range detection unit for each $\Sigma\Delta$ ADC. User can communicate with any of the ADC through SPI interface using four bits channel address. There are two modes of operation: Program mode and Flight mode. User can select any of the modes through a primary input pin. During Program Mode, user can program all the ADC cores and IDACs and during flight mode user can read the data continuously.



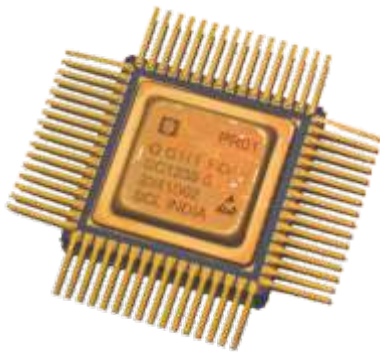
Each $\Sigma\Delta$ ADC uses a second order modulator with a Programmable Gain Amplifier (PGA) and on-chip offset and gain calibration. $\Sigma\Delta$ Modulator converts the analog input signal into a single bit stream of 1s and 0s where the density of 1s and 0s represents the digitized information. The single bit data from modulator is then processed by a digital Sinc3 filter to produce a 24 bits digital output. The output data rate of $\Sigma\Delta$ ADC is programmable. Each 8-bits current DAC is available with three different ranges: 0.5mA, 1mA and 2mA.

FEATURES:

- Sixteen $\Sigma\Delta$ ADCs
- 24 Bits resolution
- No missing code
- PGA from 1 to 128 (Binary Steps)
- Programmable Output Data Rate
- INL : 0.005%
- 19 Bits ENOB (PGA = 1, OSR=2047)
- On-chip Offset and Gain Calibrations
- Data Format Selection
- Thirty Two IDACs
- 8 Bits resolution
- Programmable Full Scale Ranges of 0.5 mA, 1mA and 2mA.
- Precision on-chip 1.22V Reference
- Accuracy: 1.7%, Drift: ± 80 ppm
- On Chip 1.8V Voltage Regulator
- Program and Flight Mode Operation
- SPI Compatible
- Supply Voltage 3.0V TO 3.6V
- 180nm SCL CMOS standard logic process
- $\theta_{JC} = 0.88^{\circ}\text{C/W}$



Octal-Core High Frequency Reconfigurable Data Acquisition System (OC HFRDAS)



DESCRIPTION:

Octal-Core High frequency Reconfigurable Data Acquisition System (OC HF RDAS) is a fully integrated data acquisition system. It incorporates 8 high resolution Sigma Delta ($\Sigma\Delta$) ADCs along with the calibration and over-range detection unit for each $\Sigma\Delta$ ADC. User can communicate with any of the ADC through SPI interface using three bits channel address. There are two modes of operation: Program mode and Flight mode. User can select any of the modes through a primary input pin. Each $\Sigma\Delta$ ADC uses a second order modulator with a Programmable Gain Amplifier (PGA). The $\Sigma\Delta$ modulator converts the analog input signal into a digital pulse train whose average duty cycle represents the digitized signal information. The pulse train is then processed by a digital sin 5 filter to produce a digital output. The output data rate of $\Sigma\Delta$ ADC is programmable.

FEATURES:

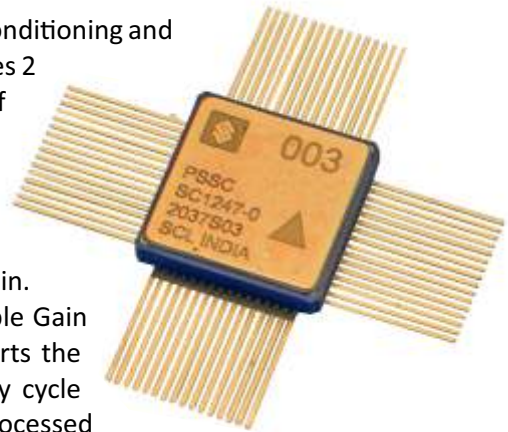
- Eight $\Sigma\Delta$ ADCs
- 24 Bits resolution
- PGA from 1 to 128 (Binary Steps)
- Programmable Data Rate
- INL : 0.01%
- 19 Bits Effective Resolution (PGA = 1, OSR=2047)
- On-chip Offset and Gain Calibrations
- Over Range Detection
- Data Format Selection
- Precision on-chip 1.22V Reference
- Accuracy: $\pm 2.5\%$, Drift: 50ppm/ $^{\circ}\text{C}$
- On Chip 1.8V Voltage Regulator
- Program and Flight Mode Operation
- SPI Compatible
- Supply Voltage : 3.0V to 3.6V
- $\theta_{JC} = 1.81^{\circ}\text{C/W}$



2 CHANNELS SIMULTANEOUS SAMPLING 24 BIT Σ - Δ ADC Pressure Sensor Signal Conditioner (PSSC)

PRODUCT DESCRIPTION:

Pressure Sensor Signal Conditioner (PSSC) is developed for signal conditioning and digital conversion of the Pressure Sensor output data. It incorporates 2 Numbers of high resolution Sigma Delta ($\Sigma\Delta$) ADCs, 2 Numbers of Eight Bits IDACs along with the calibration and over-range detection unit for each $\Sigma\Delta$ ADC. User can communicate with any of the ADC through SPI interface using one bit channel address. There are two modes of operation: Program mode and Flight mode. User can select any of the modes through a primary input pin. Each $\Sigma\Delta$ ADC uses a second order modulator with a Programmable Gain Amplifier (PGA) and on-chip offset and gain calibration. It converts the analog input signal into a digital pulse train whose average duty cycle represents the digitized signal information. The pulse train is then processed by a digital sinc3 filter to produce a digital output. The output data rate of $\Sigma\Delta$ ADC is programmable. Each 8-bits current DAC is available with three different ranges: 0.5mA, 1mA and 2mA. The device interface is SPI Compatible.



FEATURES:

- Two $\Sigma\Delta$ ADCs
- 24 Bits resolution
- PGA from 1 to 128 in binary steps
- Programmable Data Rate
- INL : 0.003%
- 19 Bits ENOB (PGA = 1, OSR=2047)
- On-chip Offset and Gain Calibrations
- Over Range Detection
- Data Format Selection
- Fully Differential Reference Inputs
- Two Offset DACs (ODACs)
- 8 Bits resolution
- Programmable up to half of full scale range at each PGA.
- Two Current DACs (IDACs)
- 8 Bits resolution
- Programmable Full Scale Ranges of 0.5mA, 1mA and 2mA.
- Precision on-chip 2.5V Reference
- Accuracy: $\pm 1\%$, Drift: $\pm 36\text{ppm}/^\circ\text{C}$
- On Chip Temperature Sensor
- Program and Flight Mode Operation
- SPI Compatible
- Supply Voltage 3.0V To 3.6V



SINGLE CHANNEL 24 BIT CAPACITANCE TO DIGITAL CONVERTER (ASC)



PRODUCT DESCRIPTION:

Accelerometer Signal Conditioner (ASC) is a Sigma Delta Modulator based high resolution Capacitance-to-Digital Converter. It senses the change in the differential capacitance connected at the input and produces a 24 Bit digital code proportional to this change. This device is developed for sensing the capacitance change of MEMS based Accelerometer and can be used in other similar applications as well. The capacitance to be sensed can be directly connected at the input of this device.

ASC incorporates a Second Order Sigma Delta ($\Sigma\Delta$) Modulator. The $\Sigma\Delta$ Modulator converts the difference in the input differential capacitors into a digital 1 bit pulse train whose average duty cycle represents the digitized signal information. The pulse train is then processed by a digital sinc3 filter to produce a digital output.

Features:

- 24 Bits No Missing Codes
- Full Scale Input Capacitance Range CFS Up To $\pm 4\text{pf}$
- Nominal Capacitance Range C0 Up To 17.75pf
- INL : 0.04%
- 18 Bits Effective Resolution
- Programmable Data Output Rates Up To 8kSPS
- On Chip Temperature Sensor
- On-chip Offset & Gain Calibration
- SPI Compatible
- 3.0v To 3.6v
- 180nm SCL Cmos Standard Logic Process
- ESD Protection Upto $\pm 3\text{kv}$ HBM



10-BIT, 1.5MSPS, SUCCESSIVE-APPROXIMATION -REGISTER (SAR) ANALOG TO DIGITAL CONVERTER

PRODUCT DESCRIPTION:

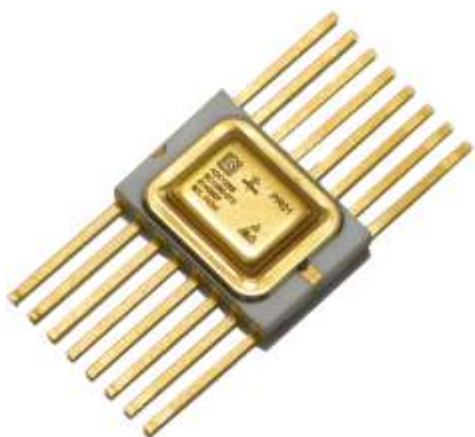
The 10-bit SAR is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 10-bit digital word up to 1.5 Mega samples per second (MSPS) in serial and parallel mode. This converter uses a SAR architecture, operating on a single 3.3V power supply, device achieves 10-bits effective resolution and consumes <5mW power. The inputs provide a full scale input swing equal 0.65V to 2.65V. Full scale input range is recommended for optimum performance. The ASIC is fabricated in 180nm SCL CMOS Standard Logic Process.

FEATURES:

- Operating Voltage: 3.3V
- Resolution: 10-Bit
- Data Rate: 1.5MSPS
- Input Range: 4Vp-p Differential Ended
- No missing code Guaranteed
- Output Data Format: Straight Binary (Serial and Parallel)
- Power Consumption < 5mW
- SCL's 180nm CMOS Technology
- Operating Temperature (TA): -55°C to +125°C
- Packaged in 64 Pins CQFP



12-BIT, 1MSPS, 7-CHANNEL SUCCESSIVE-APPROXIMATION-REGISTER (SAR) ANALOG TO DIGITAL CONVERTER



PRODUCT DESCRIPTION:

The SC1260-0T2 device is a low-power; seven channel CMOS 12-bit Successive Approximation analog-to-digital converter specified for conversion throughput rates of 50kSPS to 1MSPS. The converter is based on successive approximation register architecture with an internal track-and-hold circuit. The device can be configured to accept up to seven input signals at inputs IN0 through IN6 and performs a 12-bit successive approximation analog-to-digital conversion in a nominal period of 16 clock cycles. The output serial data is straight binary and is compatible with serial interfaces. The 12-bit digital output has a tri-state control allowing the connection of multiple SC1260-0T2. This provides the ability to interface many sensor voltage readings to the digital processor data bus. The full-scale range is determined by analog supply voltages. The analog supply (VA) can range from 3.0 V to 3.3V, and the digital supply (VD) can range from 3.0 V to VA. Normal power consumption using a 3.3V supply is < 20mW for 16MHz SCLK and <7mW for 1MHz SCLK.

FEATURES:

- Resolution: 12Bits
- Sampling Frequency: 50KSPS to 1MSPS
- No missing code Guaranteed
- Output Data Format :Straight Binary
- Operating Voltage: 3.3V
- Power Consumption < 20mW for 16MHz SCLK and <7mW for 1MHz SCLK
- Input Range :3.3V Single Ended
- Package: 16 Lead Flat Package
- $\theta_{jc}=7.1^{\circ}$ C/W
- Technology: 180nm SCL CMOS Standard Logic Process -55°C to +125°C
- Packaged in 48 Pin CFP



12-BIT 200 MSPS CURRENT STEERING DAC (Digital to Analog Converter)

PRODUCT DESCRIPTION:

The SC9023-0 is integrated 12-bit 200MSPS digital-to-analog converter with a tunable full-scale output current from 2mA to 20mA and having two complementary outputs. It has an on-chip precise low drift voltage reference of 1.2V. SC9023-0 can also operate with an external reference. This may improve the DC accuracy if the external reference circuitry is superior in its drift and accuracy. Latches are provided for high-speed synchronization providing better AC characteristics for DAC. The ASIC is fabricated in 180nm SCL CMOS technology.



FEATURES:

- Operating Voltage: 3.3V/1.8V
- Resolution: 12Bits
- Data Rate: 200MSPS
- Full Scale Current: 2mA to 20mA
- On Chip Voltage References
- Input straight Binary Format
- Package: 64 PIN CQFP
- Radiation hardened (TID) up to 300Krad(Si)



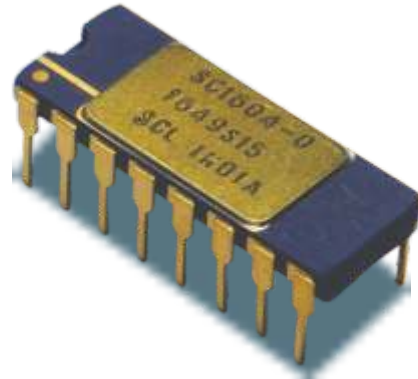
INTERFACE, SUPERVISORY, AMPLIFIERS & DRIVERS



RS422 TRANSCEIVER

PRODUCT DESCRIPTION:

RS422 (SC1604-0) is a low power differential line transceiver designed for multi-point data transmission standard RS422 applications. The CMOS design offers significant power saving over its bipolar counterpart without sacrificing ruggedness against ESD damage. It offers a choice of active-high or active-low inputs. The device is designed for line/bus transmission at switching rates up to 5 MHz. The device can operate over a large temperature range -55°C to +125°C and it is packaged in ceramic-16 pin package.

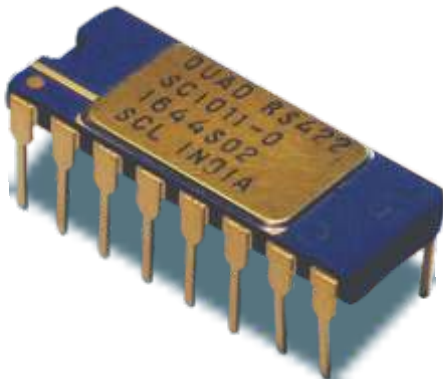


FEATURES:

- Operates from Single 3.3V V_{CC}
- Integrated 3.3V to 1.8V linear voltage regulator
- Switching Rates up to 5 MHz
- Transmission Rate up to 10 Mbps
- Receiver input sensitivity of 400mV guaranteed over the entire power supply range
- Designed for RS422 applications
- Fail safe feature guarantees high output state when receiver inputs are left open
- Common Mode Output Voltage Range: 0V to 3V
- SCL's 180nm CMOS Technology



QUAD RS422 DRIVER



PRODUCT DESCRIPTION:

Quad RS-422 (SC1011-0) is a differential line driver that operates with a 3.3V power supply. The enable function is common to all four drivers and offers a choice of active-high or active-low inputs. Each driver has a separate input and output pins for full-duplex bus communication designs. The device is designed for balanced bus transmission at switching rates up to 5 MHz. The device can operate over a large temperature range -55°C to +125°C and it is packaged in ceramic-16 pin package.

FEATURES:

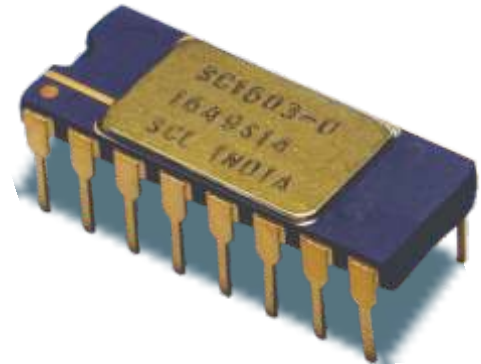
- Operates from Single 3.3V V_{cc}
- Switching Rates up to 5 MHz
- Transmission Rate up to 10 Mbps
- Differential-State Outputs
- Designed for Multipoint Bus Transmission
- Common Mode Output Voltage Range: 0V to 3V
- SCL's 180nm CMOS Technology



RS485 TRANSCEIVER

PRODUCT DESCRIPTION:

RS485 (SC1603-0) is a low power differential line transceiver designed for multi-point data transmission standard RS485 applications. The enable function is different for both transmitter and receiver lines. It offers a choice of active- high or active-low inputs. The device is designed for line/bus transmission at switching rates up to 5 MHz. The device can operate over a large temperature range -55°C to +125°C and it is packaged in ceramic-16 pin package.



FEATURES:

- Operates from Single 3.3V V_{cc}
- Integrated 3.3V to 1.8V linear voltage regulator
- Switching Rates up to 5 MHz
- Transmission Rate up to 10 Mbps
- Receiver input sensitivity of 200mV guaranteed over the entire power supply range
- Designed for RS485 applications
- Fail safe feature guarantees high output state when receiver inputs are left open.
- Common Mode Output Voltage Range: 0V to 3V
- SCL's 180nm CMOS Technology



Addressable Synchronous/Asynchronous Differential Receiver (ASDR)



DESCRIPTION:

ASDR (Addressable Synchronous / Asynchronous Differential Receiver) is a mixed signal ASIC being developed under Technology Development Project (TDP). It has three RS422 differential receivers, one RS422 differential transmitter, Digital Serial to Parallel Converter, on chip oscillator, Linear Voltage Regulator (LVR) and power on reset circuit.

The ASIC takes up to three RS422 differentials inputs and convert it into 16 bit CMOS parallel Signal with different modes.

Mode-0: synch 24 bit data, with a strobe width of 24 bit

Mode-1: synch 24 bit data, with a strobe width of 1 bit

Mode-2: synch 16 bit data, with gated clock

Mode-3: asynchronous 8 bit UART

FEATURES:

- Synchronous / Asynchronous serial (RS422) to parallel converter with different modes.
- 4 Operating Mode (3 Synchronous and 1 Asynchronous)
- 5Bit Local Address
- 10 Mbps Speed (as per RS422 Std.)
- Common Mode Voltage: 0.5 V to 2.7V
- RS 422 Input Sensitivity: 0.2V to 3.3V
- On Chip Oscillator: 3.12 MHz
- On Chip LVR: 1.8V \pm 4%, 50mA
- Operating Temperature: -55°C to +125°C
- Power Supply: AV_{DD}-3.3V, DV_{DD}- 1.8V
- Current Consumption: \leq 10mA

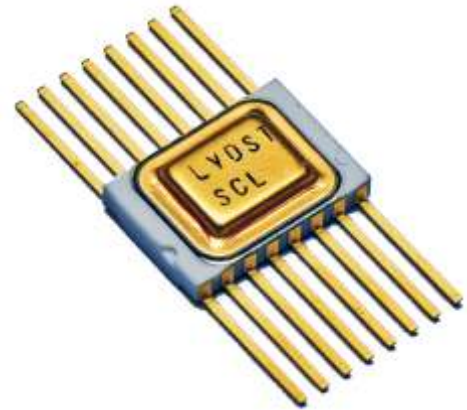


High Speed Quad LVDS Driver

PRODUCT DESCRIPTION:

The SC1002-1 is a quad, low-voltage, differential signalling (QLVDS) driver specifically designed in a low-power and fast point-to-point baseband data transmission standard.

The intended application of these devices and signalling technique is point-to-point data transmission over controlled impedance media of approximately 100 ohm. The transmission media may be printed-circuit board traces, backplanes or cables.



FEATURES:

- Single Power Supply 3.3V \pm 0.3V
- LVTTTL/CMOS logic input levels and LVDS output levels
- 400 Mbps (200 MHz) switching rates
- \pm 350 mV differential signalling
- Power dissipation 26 mW Typical per driver at 200 MHz (VDD=3.3V)
- Propagation delay \leq 5 nsec.
- Compatible with ANSI/TIA/EIA-644 LVDS standard
- Operating Temperature (T_A): -55°C to +125°C
- Driver output at high impedance when disabled or with VDD = 0
- Cold sparing at LVDS output pins.
- Pin compatible with QLVDS driver LVDS31
- ESD protection upto class-1 (< 1999V)
- Latch up current protection up to \pm 100mA
- Hermetic sealed 16 pin Flat package
- Package Θ_{jc} = 3.1°C/Watt
- SCL's 180nm CMOS Technology



High Speed Quad LVDS Receiver



PRODUCT DESCRIPTION:

The SC1003-1 is a quad, low-voltage, differential signalling (QLVDS) line receiver specifically designed in a low-power and fast point-to-point baseband data transmission standard.

Any of the four differential receivers provides a valid logical output state with a $\pm 100\text{mV}$ differential input voltage within the input common-mode voltage range. The circuit features an internal fail safe function to ensure a known output state in case of an input short circuit or floating. The intended application of these devices and signalling technique is point-to-point data transmission over controlled impedance media of approximately 100 ohm. The transmission media may be printed-circuit board traces, backplanes or cables.

FEATURES:

- Single Power Supply $3.3\text{V} \pm 0.3\text{V}$
- LVDS input levels and CMOS logic output levels
- 400 Mbps (200 MHz) switching rates
- Differential input thresholds $\pm 100\text{mV}$
- Open circuit fail safe function
- Power dissipation 76 mW Typical per receiver at 200MHz (VDD=3.3V)
- Propagation delay $\leq 5\text{ nsec.}$
- Compatible with ANSI/TIA/EIA-644 LVDS standard
- Operating Temperature (TA): -55°C to $+125^\circ\text{C}$
- Cold Sparring at LVDS input pins
- Pin compatible with QLVDS receiver LVDS33
- ESD protection upto class 1 ($< 1999\text{V}$)
- Latch up current protection $\pm 100\text{mA}$
- SCL's 180nm CMOS Technology
- 16-Pin Ceramic-Dual-Flat package
- Package $\Theta_{\text{JC}} = 3.1^\circ\text{C/Watt}$
- FM Qualified as per MIL STD 883

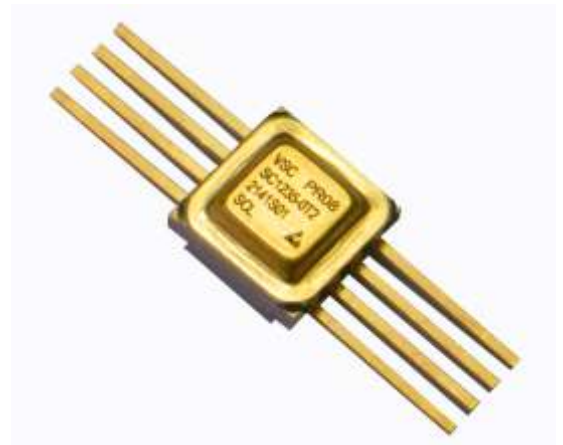


3.3V Voltage Supervisory Circuit

PRODUCT DESCRIPTION:

This device is a 3.3V supervisory circuit that reduces the complexity required to monitor supply voltage in microprocessor systems. This device will significantly improve accuracy and reliability relative to discrete solutions. This device has following key functions

- A reset output during power-up, power down and brownout conditions
- A precision threshold voltage detector for monitoring a power supply.
- An active-low, manual-reset input.



FEATURES:

- Analog Supply Voltage is 3.3V
- Precision Supply Voltage Monitor: 3.195 V Threshold
- Reset Pulse Width 178ms (typical)
- Precision threshold detector 0.61V threshold
- Operating Temperature (T_A): -55°C to +125°C
- Low Power Dissipation.
- Packaged in 8-Pin CFP package.
- SCL's 180nm CMOS Technology



Quad Core Charge to Voltage Amplifier (QCCVA)



PRODUCT DESCRIPTION:

Charge Amplifier is a signal conditioner which conditions the signal from Vibration, Shock and Acoustic transducers. Quad Core Programmable C-to-V Amplifier (EF1008-0) contains 4 cores of programmable C-to-V amplifier. Each of the cores can be programmed independently through input control signals. The user can select any of the gain and DC output value by applying the appropriate value at the control inputs.

Programmable C-to-V amplifier is targeted for vibration, acoustic and other measurements having charge as input. The device converts input charge to voltage. Charge to Voltage converter is followed by the Programmable Gain Amplifier (PGA) which provides 6 programmable gains from 1 to 32 binary steps. The DC level of the output is shifted up to four different values. The user can set the values of PGA and DC output level using input control signals.

FEATURES:

- Analog Supply Voltage is 5V.
- Digital Supply is 3.3V.
- PGA: 1 to 32 in Binary Steps.
- Output DC level Adjustment: 0, 1.25, 1.65 and 2.5 Volt.
- Operating Temperature (T_A): -55°C to +125°C
- Low Power Dissipation.
- Packaged in 64 Pin CQFP package.



Capacitance-to-digital Converter (CDC)

PRODUCT DESCRIPTION:

SC1602 is a high resolution, Sigma Delta based Capacitance-to-digital Converter (CDC). The capacitance to be measured is connected directly to the device inputs. The device also offers offset and non-linearity correction (upto second order) of the sensors with capacitances upto 28pf. It can also accept upto 28pf common mode capacitance. It is designed for single ended capacitive sensors (both terminals must be available). The serial interface is SPI compatible.

CDC is operated with supply of analog voltage 3.3 V and digital voltage 1.8 V across the temperature range of -40°C to +125°C.

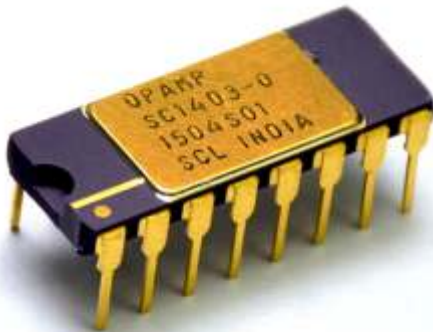


FEATURES:

- 12-bit resolution
- Wide Capacitance range of 4 pf to 28 pf.
- Input offset capacitance range of 4 pf to 28 pf.
- Programmable output data rate of upto 4 KHz.
- SPI compatible serial interface.
- Non-linearity correction of sensor (up to 2nd order)



OPERATIONAL AMPLIFIER



PRODUCT DESCRIPTION:

Operational amplifier (SC1403-0) is designed as an IP block. This chip consists of 2 nos. of internally compensated CMOS input op-amps in folded cascade architecture. First op-amp has internal bias resistor whereas second op-amp requires approx. 33k Ω external bias resistor.

FEATURES:

- Open loop Gain > 80db
- Settling Time (0.05%) < 40ns
- Unity Gain Bandwidth > 32MHz
- Supply: $\pm 1.65\text{V}$ (Dual supply) +3.3V (single supply)
- Power Dissipation < 15mW
- Slew Rate: 70 V/ μs
- Input offset voltage $\pm 6.7\text{mV}$
- Offset voltage drift 4 $\mu\text{V}/^\circ\text{C}$
- Load Resistance > 1K Ω
- Test Circuit
- Load Capacitance < 30pF
- SCC 180nm CMOS Technology



INSTRUMENTATION AMPLIFIER

PRODUCT DESCRIPTION:

Programmable Current feedback instrumentation amplifier (SC1406-0) is an IP based solution for high CMRR applications of the order of 80db and above. The output voltage swing is completely independent of input common mode voltage. It has six independent closed loop gain options which can be selected through two control lines. It offers Single supply operation and consumes low power.

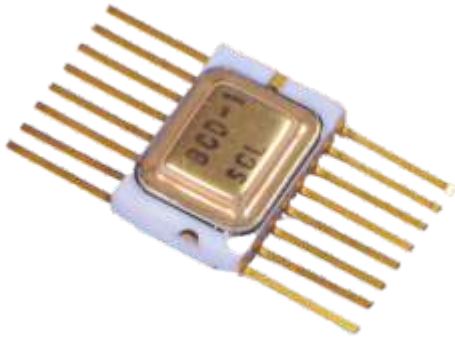


FEATURES:

- 3.3V single power supply
- CMOS logic input levels for digital I/O
- Low power dissipation ($< 2\text{mW}@3.3\text{Vstatic}$)
- Minimum CMRR: 87.6dB (DC)
- Minimum CMRR: 66dB at 10KHz
- Minimum PSRR: 63.20 dB
- Minimum PSRR: 54.58 dB at 1KHz
- High Input Impedance
- Bandwidth (G=1): 1.13MHz
- Six programmable gain option
- Operating Temperature: -55°C to $+125^{\circ}\text{C}$
- SCL's 180nm CMOS Technology
- Hermetic sealed 14 pin DIP



SINGLE CHANNEL, 5MHz, 850pF, BIPOLAR CLOCK DRIVER



PRODUCT DESCRIPTION:

The EF1103-0 is a high-speed clock driver specifically designed and packaged in a hermetic sealed ceramic flat-16 lead (SOP) package for use in high speed CCD and time delay integration (TDI) detector clocks. The intended application of these devices is to drive high capacitive CCD loads of the order of $\sim 850\text{pF}$ and fast rise / fall requirements.

FEATURES:

- 3.3V power supply for VDD
- 5 MHz operating frequency
- Single channel input
- Input level shifters
 $5\text{V} \geq V_L \geq -5\text{V}$
 $9\text{V} \leq V_H \leq 14\text{V}$
- Low power dissipation (0.7W at 5MHz with output load of 850pf)
- $20\text{ns } t_R/t_F$ at 850pF load
- $30\text{ns } T_{PLH}/T_{PHL}$ delay
- Matched rise and fall time $< 2\text{ns}$
- Matched propagation delay match $< 2\text{ns}$
- 16 pin Lead Flat package (SOP)
- Operating Temperature: -55°C to $+125^\circ\text{C}$

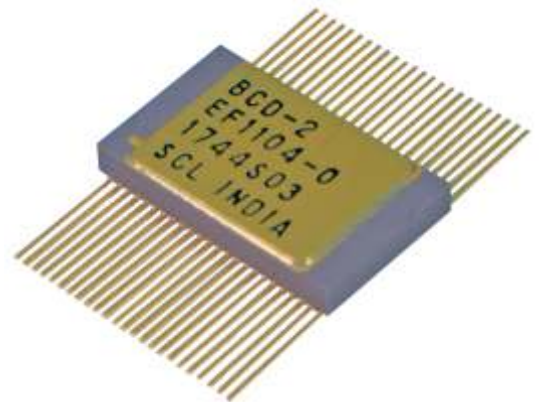


FOUR CHANNEL, 5MHz, 850pF, BIPOLAR CLOCK DRIVER

PRODUCT DESCRIPTION:

The EF1104-0 is a high-speed clock driver specifically designed and packaged in a hermetic sealed ceramic flat-48 lead DIL package for use in high speed CCD and time delay integration (TDI) detector clocks.

The intended application of these devices is to drive high capacitive CCD loads of the order of ~850pF and fast rise / fall requirements.

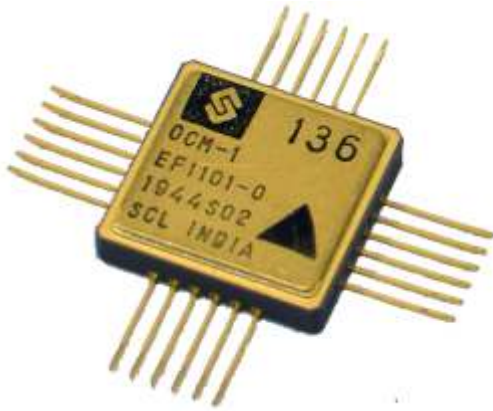


FEATURES:

- 3.3V power supply for VDD1
- 5 MHz operating frequency
- Four channel input
- Input level shifters
 - $5V \geq V_L \geq -5V$
 - $9V \leq V_H \leq 14V$
- Low power dissipation (5W at 5MHz with output load of 850pf on each output)
- 15ns t_r/t_f at 850pF load
- 25/27 ns T_{PLH}/T_{PHL} delay
- Matched rise and fall time <2ns
- Matched propagation delay match <3ns
- Hermetic sealed 48 pin Lead Flat package (DIL)
- Operating Temperature: -55°C to +125°C



FOUR CHANNEL, 5MHz, 3000pF, CLOCK DRIVER



PRODUCT DESCRIPTION:

The FT CCD detectors are envisaged to use in high-resolution application designs. Detector clocks requirements for external TDI operation are more complex due to large capacitive drive requirements. The clock drivers need to drive a high capacitive load $\sim 3000\text{pF}$. A 4 channel clock driver having one 3000pF , one 150pF , one 50pF , and one 25pF channel driving capabilities has been developed.

FEATURES:

- 3.3V power supply for VDD1
- 5 MHz operating frequency
- Four channels input
- Input level shifters
 - $0.6\text{V} \geq \text{VL} \geq 0\text{V}$
 - $12\text{V} \leq \text{VH} \leq 14\text{V}$
- Low power dissipation ($<4\text{W}$ at 5MHz)
- $t_r=50\text{ns}$, $t_f=44\text{ns}$ at 3000pF load
- $t_r=5\text{ns}$, $t_f=6\text{ns}$ at 150pF load
- $T_{\text{PLH}} = 24\text{ns}$, $T_{\text{PHL}} = 25\text{ns}$ delay
- Matched rise and fall time $<7\text{ns}$
- Matched propagation delay match $<2\text{ns}$
- Hermetic sealed 16 pin Quad flat package
- Operating Temperature: -55°C to $+125^\circ\text{C}$
FM Qualified as per MILSTD 883
FT CCD Imager for OCM-III

This device is successfully used in OCM payload of Oceansat-III mission.



TWELVE CHANNEL, 1MHz, 3000pF, CLOCK DRIVER

PRODUCT DESCRIPTION:

The FT CCD detectors are envisaged to use for high-resolution application designs. Detector clocks requirements for external TDI operation are more complex due to large capacitive drive requirements. The clock drivers need to drive a high capacitive load $\sim 3000\text{pF}$. A 12 channel clock driver having four 3000pF channel and eight 150pF channel driving capabilities has been developed.

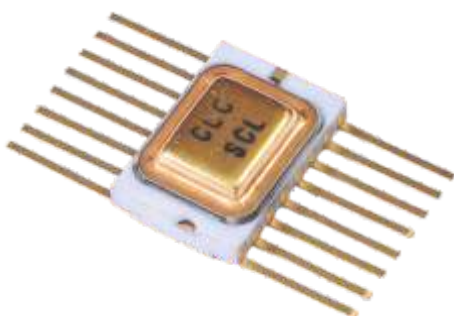


FEATURES:

- 3.3V power supply for VDD1
- 1 MHz operating frequency
- Twelve channels input
- Input level shifters
 - $0.6\text{V} \geq V_L \geq 0\text{V}$
 - $12\text{V} \leq V_H \leq 14\text{V}$
- Low power dissipation ($<5\text{W}$ at 1MHz)
- $t_R=60\text{ns}$, $t_F = 5 \text{ ns}$ at 3000pF load
- $t_R=6\text{ns}$, $t_F = 7 \text{ ns}$ at 150pF load
- $T_{PLH}=26\text{ns}$, $T_{PHL}=27\text{ns}$ delay
- Matched rise and fall time $<7\text{ns}$
- Matched propagation delay match $<2\text{ns}$
- Hermetic sealed 64 pin Ceramic Quad Flat package
- Operating Temperature: -55°C to $+125^\circ\text{C}$



FOUR CHANNEL, 5MHz, 1000pF, CLOCK DRIVER



PRODUCT DESCRIPTION:

The EF1105-0 is a high speed non-inverting, quad CMOS driver. It is capable of running at clock rates up to 5 MHz and features 0.6A typical peak drive capability and a nominal on-resistance of just 3Ω . The EF1105-0 is ideal for driving highly capacitive loads, such as storage and vertical clocks in CCD applications. It is also well suited to ATE pin driving, level-shifting, and clock-driving applications. Each output can be switched to either the high (VH) or low (VL) supply pins, depending on the related input pin. The inputs are compatible with both 3V and 5V CMOS and TTL logic. The output enable (OE) pin can be used to put the outputs into a high-impedance state. This is especially useful in CCD applications, where the driver should be disabled during power down. The driver has fast rise and fall times, which are typically matched to within 20ns (for $C_{Load}=1nF$). The ceramic flat pack (16 Lead) is taken for packaging.

FEATURES:

- 5 MHz operating frequency
- Wide output voltage range
- Four channels input
- Input level shifters
$$8V \geq VL \geq -5V$$
$$0V \leq VH \leq 15V$$
- Low power dissipation (5W at 5MHz with output load of 1000 of on each output)
- $t_R = 22ns, t_F = 20ns$ @ 1000pf load
- $t_{PLH} = 38ns, t_{PHL} = 41ns$ delay @ 1000pf load
- Matched rise and fall time $< 3ns$
- Matched propagation delay match $< 4ns$
- Peak drive, 0.6A
- On-resistance, 3Ω
- TTL/CMOS input-compatible
- 16 pin Ceramic Dual Flat package
- Operating Temperature: $-55^\circ C$ to $+125^\circ C$



STANDARD DIGITAL DEVICES



HEX BUFFER SCL4050



PRODUCT DESCRIPTION:

SC1013-0 is non-inverting hex buffer. It consists of 6 buffer stages, providing high noise immunity and a stable output. The device can operate over a large temperature range from -55°C to +125°C. Device is packaged in a hermetic sealed 16-pin ceramic dual Flat pack.

FEATURES:

- Power Supply Voltage 2.5V to 5.5V
- Cold Sparing feature at inputs
- Typical Propagation Delay: 5ns at VDD=5.0V, CL=30pF, TA=25°C
- Low Power Dissipation, $I_{DD} (typ.) < 1\mu A$
- Balanced Propagation Delays and transition times
- Symmetrical Output loading $I_{OH} = I_{OL} = 8mA$
- Operating Temperature: -55°C to 125°C.
- Pin compatible with 54HC4050
- Package $\theta_{JC} = 3.1^{\circ}C/Watt$
- 16-Pin Ceramic-Dual-Flat package
- SCL's 180nm CMOS Technology



OCTAL BUFFER SCL541

PRODUCT DESCRIPTION:

SC9029-0 is radiation hardened non-inverting Octal buffer / Line driver have three state output. The output enable pins (OE1 and OE2) control the three-state outputs. If either enable signal is high the outputs will be in the high impedance state. For data output both enables (OE1 and OE2) must be low.



FEATURES:

- Power Supply Voltage $5V \pm 0.5V$
- Cold Sparing feature at Input pins
- Three state outputs
- Low Power Dissipation, $I_{DD} (\text{Max.}) < 1\text{mA}$
- Balanced Propagation Delays. $T_{PLH} = T_{PHL}$
- Symmetrical Output Impedance
- $I_{OH} = I_{OL} = 8 \text{ mA}$
- Operating Temperature: -55°C to 125°C .
- Pin compatible with HC541
- 20 Pin Ceramic-Dual-Flat package
- SCL's 180nm CMOS Technology





16 BIT BUFFER 3-STATE OUTPUT



PRODUCT DESCRIPTION:

SC1004-2 16-bit buffer and line driver is designed for low-voltage ($V_{DD} = 3.3V$) operation, these devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. The outputs, which are designed to source or sink up to 7mA, include equivalent small series resistors to reduce overshoot and undershoot. zActive bus-hold circuitry holds unused or undriven inputs at a valid logic state. These devices are fully specified for hot-insertion applications using IOFF and power-up 3-state. The IOFF circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FEATURES:

- Single Power Supply $3.3V \pm 0.3V$
- Cold sparing feature at I/O
- Output Ports Have Equivalent 22-W Series Resistors, so No External Resistors are required.
- 5V tolerant inputs for interfacing 5V logic with 3.3V VDD
- IOFF and power-up 3-state support hot Insertion
- Bus Hold on data inputs eliminates the need for external pull-up/pull-down resistors
- Distributed VDD and GND pins minimize high-speed switching noise
- Flow-through architecture optimizes PCB layout
- Output loading 7 mA
- 6.5 ns typical propagation delay
- Low power dissipation ($< 2mW$ at 3.6V static)
- Operating Temperature: $-55^{\circ}C$ to $125^{\circ}C$.
- Device packaged in hermetic sealed 48 pin Ceramic Dual Flat package.
- Pin compatible with 16 Bit Buffer LVTH162244.
- Package $\Theta_{jc} = 2.7^{\circ}C/Watt$
- SCL's 180nm CMOS Technology



16 BIT TRANSCEIVER 3-STATE OUTPUT

PRODUCT DESCRIPTION:

SC1124-0 16-bit Transceiver is designed for low-voltage (VDD=3.3V) operation, but with the capability to provide a TTL interface to a 5V system environment. These devices can be used as two 8-bit Transceivers or one 16-bit Transceiver.

The outputs, which are designed to source or sink up to 10 mA, include equivalent 22-W series resistors to reduce overshoot and undershoot. Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pull down resistors with the bus-hold circuitry is not recommended. These devices are fully specified for hot-insertion applications using Ioff and power-up 3-state. The IOFF circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

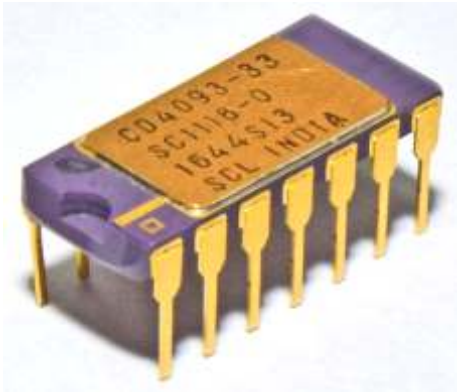


FEATURES:

- 3.3V power supply for core and I/O pads
- Cold sparing feature at I/O
- Output Ports Have Equivalent 22-W Series Resistors, so No External Resistors are required.
- 5V tolerant inputs for interfacing 5V logic with 3.3V VDD
- IOFF and power-up 3-state support hot Insertion
- Bus Hold on data inputs eliminates the need for external pull-up / pull-down resistors
- Output loading more than 7 mA
- 6.2 ns typical propagation delay
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at VDD = 3.3 V, $T_A = 25^\circ\text{C}$
- Low power dissipation <2mW at 3.6V static
- Operating Temperature: -55°C to 125°C .
- Pin compatible with 16 Bit Buffer LVTH162245.
- Package $\Theta_{JC} = 2.7^\circ\text{C/Watt}$
- SCL's 180nm CMOS Technology
- Qualified as per MIL STD 883



3.3V QUAD 2-INPUT NAND GATE SCL4093



PRODUCT DESCRIPTION:

SC1118-0 is a Quad Two input NAND gate with Schmitt trigger action on both inputs. Schmitt trigger is a comparator which triggers at different points for positive and negative going signals and the difference between positive voltage (V_{T+}) and negative voltage (V_{T-}) is the Hysteresis voltage (V_H). All outputs have equal source and sink currents.

FEATURES:

- Operating Voltage $3.3V \pm 0.3V$
- Schmitt-trigger on each input with no external components.
- Noise immunity greater than 50%
- Equal source and sink currents
- No limit on input rise and fall time
- Hysteresis voltage (any input), $V_H = 0.8V$ ($V_{DD} = 3.3V$ and $T_A = 25^\circ C$)
- $T_A = 25^\circ C$ (Typical)
- $V_{DD} = 3.3V$, $V_H = 0.8V$
- Operating Ambient Temperature: $-55^\circ C$ to $125^\circ C$
- 14 pin ceramic Dual in line package / Ceramic Flat package
- Pin compatible with CD4093
- Package $\Theta_{JC} = 7.17^\circ C/Watt$
- SCL's 180nm CMOS Technology
- Qualified as per MIL STD 883



5V QUAD 2-INPUT NAND GATE SCL4093

PRODUCT DESCRIPTION:

SC1125 is a Quad Two input NAND gate with Schmitt trigger action on both inputs. Schmitt trigger is a comparator which triggers at different points for positive and negative going signals and the difference between positive voltage (V_{T+}) and negative voltage (V_{T-}) is the Hysteresis voltage (V_H). All outputs have equal source and sink currents.



FEATURES:

- Operating Voltage $5V \pm 0.5V$
- Schmitt-trigger on each input with no external components.
- Noise immunity greater than 50%
- Equal source and sink currents
- No limit on input rise and fall time
- Hysteresis voltage (any input) $V_H = 1.6 V$ ($V_{DD} = 5.05$ and $T_A = 25^\circ C$)
- Operating Ambient Temperature: $-55^\circ C$ to $125^\circ C$
- 14pin ceramic flat package (CSOP)
- Pin compatible with CD4093
- Package $\Theta_{JC} = 7.17^\circ C/Watt$
- SCL's 180nm CMOS Technology



3.3V HEX SCHMITT TRIGGER INVERTER SCL5414



PRODUCT DESCRIPTION:

SC1111-0 is a hex inverter with Schmitt trigger action on inputs. Schmitt trigger is a comparator which triggers at different points for positive and negative going signals and the difference between positive voltage (V_{T+}) and negative voltage (V_{T-}) is the Hysteresis voltage (V_H). All outputs have equal source and equal sink currents.

FEATURES:

- Operating Voltage $3.3V \pm 0.3V$
- Schmitt-trigger on each input with no external components.
- Noise immunity greater than 50%
- No limit on input rise and fall time
- Hysteresis voltage (any input) $V_H = 1.04V$ ($V_{DD} = 3.3V$ and $T_A = 25^\circ C$)
- Operating Ambient Temperature $-55^\circ C$ to $125^\circ C$
- 14-pin ceramic flat package (SOP) Pin compatible with 5414
- SCL's 180nm CMOS Technology
- Qualified as per MIL STD 883



5V HEX SCHMITT TRIGGER INVERTER SCL5414

PRODUCT DESCRIPTION:

SC1126-0 is a Hex Inverter with Schmitt trigger action on all inputs. Schmitt trigger is a comparator which triggers at different points for positive and negative going signals and the difference between positive voltage (VTP) and negative voltage (VTN) is the Hysteresis voltage (VH).



FEATURES:

- Operating Voltage $5.0V \pm 0.5V$
- Schmitt-trigger on each input with no external components.
- Cold sparing feature available at input pins
- Noise immunity greater than 50%
- No limit on input rise and fall time
- Hysteresis voltage (any input) $V_H = 1.1V$ ($V_{DD} = 5.0V$ and $T_A = 25^\circ C$)
- Operating Ambient Temperature: $-55^\circ C$ to $125^\circ C$
- 14-pin ceramic flat package (SOP) Pin compatible with 5414
- SCL's 180nm CMOS Technology
- Qualified as per MIL STD 883



8-CH ANALOG MUX DEMUX SCL4051



PRODUCT DESCRIPTION:

The SC1018-0T1 is an 8-channel analog multiplexer demultiplexer with three address inputs (S0 to S2), an active LOW enable input (\bar{E}), eight independent inputs/outputs (Y0 to Y7) and a common input/output (Z). The device contains eight bidirectional analog switches, each with one side connected to an independent input/output (Y0 to Y7) and other side connected to a common input/output (Z). VDD and VSS are the supply voltage connections for the digital control inputs (S1 to S3, and \bar{E}). The analog inputs/outputs (Y0 to Y7, and Z) can swing between VDD as a positive limit and VSS as negative limit.

FEATURES:

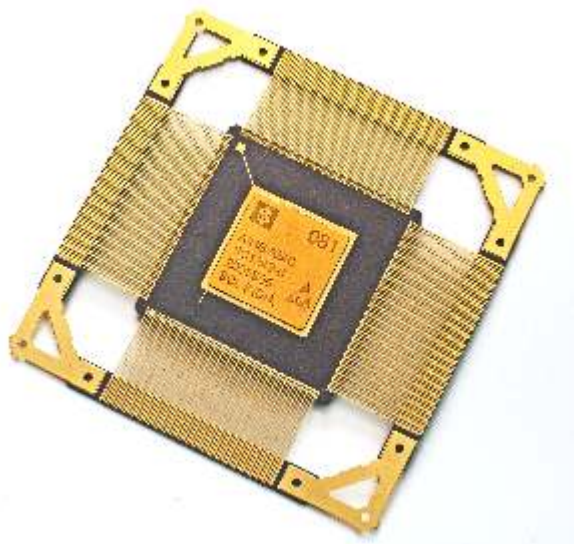
- 5V power supply for core and I/O pads
- Fully static operation.
- Low on resistance i.e. 200 ohm (Typ.)
- Low power dissipation (< 1uW at 5V static)
- Operating Ambient Temperature -55°C to 125°C
- 16 pin ceramic flat package (CSOP)
- Pin compatible with CD4051
- Package $\Theta_{jc} = 3.1$ °C/Watt
- SCL's 180nm CMOS Technology



APPLICATION SPECIFIC INTEGRATED CIRCUIT ASICs



ACTUATOR INTERFACE AND HEATER SWITCHING (AIHS) – ASIC3



PRODUCT DESCRIPTION:

The main functions of this ASIC are to provide interfaces for Heater Switching Logic and Isolation Latch Valve Interfaces. As this ASIC has to be interfaced with the processor, it includes necessary interface logics for this purpose also. The required functionalities are segregated into four main logic blocks. All the Input and Output signals are routed through de-multiplexers appropriately, using function select signals SEL [1:0].

FEATURES:

- Single Supply Operation $5V \pm 0.5V$
- Max. Operation Frequency 25 MHz
- Quiescent Supply Current 1 mA
- Output loading 12 mA
- Operating Temperature -55°C to 125°C
- Testability Features: Scan and Functional
- Packaged in 256 Pins, CQFP
- SCL's 180nm CMOS Technology
- Qualified as per MIL STD 883

The Radiation Hardened ASIC 3 developed at SCL facility will be used extensively in the Satellite sub-systems of the Spacecraft replacing the imported devices. This device was used in On-board Spacecraft of RISAT-2BR2 & planned for future missions of ISRO.



PROGRAMMABLE DIGITAL BPSK DEMODULATOR & BIT SYNCHRONIZER (ASIC-10)

PRODUCT DESCRIPTION:

ASIC-10 is a programmable digital BPSK demodulator & Bit synchronizer required in telecommand system to perform the function of demodulation and bit synchronization at data rates starting from 100 BPS to 16 KBPS. Digital Demodulator uses Costas Loop for demodulation and Bit Synchronizer uses In phase/ Mid Phase Shift Keying (also called as Data Transition Tracking Loop (DTTL)) algorithms. Binary Phase Shift Keying (BPSK), in terms of noise immunity per unit bandwidth, is one of the most efficient binary data modulation techniques.



FEATURES:

- Single Supply Operation 5V±0.5V
- Operation Frequency 26.31 MHz
- Inputs can be left floating (pulled up internally)
- Quiescent Supply Current 5.3 mA
- Output loading 4 mA
- Operating Temperature -55°C to 125°C
- Testability Features: Scan and Functional
- Packaged in 132 Pins, CQFP
- SCL's 180nm CMOS Technology

The indigenized developed device will be used in satellite Tele-Command sub system.



CMOS CAMERA CONFIGURATION ASIC



PRODUCT DESCRIPTION:

This ASIC is the part of “Miniature Camera System”, based on a commercial off-the- shelf (COTS) camera module. The COTS Camera module consists of optics, sensors and has versatile features such as HD resolution, integrated digitizer, signal processing electronics, inbuilt JPEG compression etc. This camera requires clock as control signal and I2C bus signals for its configuration in addition to supply for its operation. The camera outputs 8-bit parallel data along with frame and line sync signals and a pixel clock. Therefore, it requires a host module which can cater to provide configuration bits to control the camera and also take output from it for further processing.

FEATURES:

- Single Power Supply, 3.3V±10%
- Option for both single ended & differential clock inputs
- Four mode selection bits enables sixteen Camera configuration modes
- Operating frequency of 70 MHz
- Operating Temperature -55°C to 125°C
- Package: 64 lead Cer-Quad (z-type)
- SCL's 180nm CMOS Technology
- Qualified as per MIL STD 883

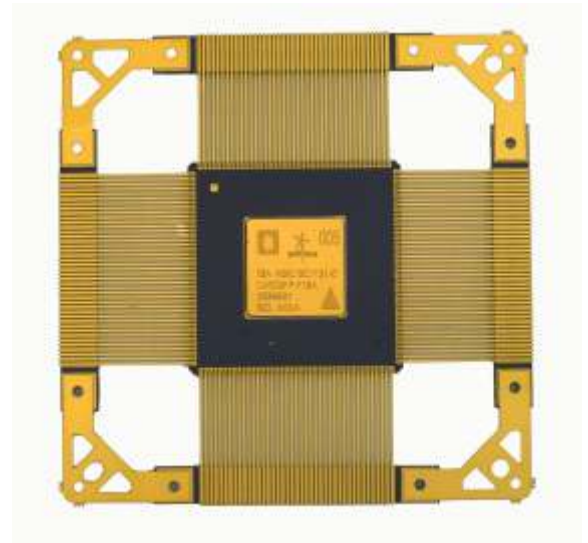
The device integrated into the Lander has flown as part of the 'Miniature Camera System' in Chandrayaan-II & Chandrayaan-III Missions.



INERTIAL SENSOR ACQUISITION ASIC (ISA)

PRODUCT DESCRIPTION:

ISA ASIC is an interface controller between ISU system and processor. ISA ASIC is used to acquire functional and health monitoring parameters from the sensors and store the data in receive buffers for the processor to read. ISA is to be designed as a memory peripheral to the main processor. The external interfaces are to be controlled by writing into specific configuration registers in ISA. ISA supports ISU interfaces such as UART links, analog data acquisition, NAVIC UART link interface, counters for VFC output and mode command/demag PWM for system powering sequence.



FEATURES:

- 3.3 V I/O pads Power Supply
- 1.8 V Core Supply
- Operation Frequency 50 MHz
- Quiescent Supply Current < 1mA
- Output loading ± 4 mA
- Operating Temperature -55°C to 125°C
- Testability Features: Scan and Functional
- Packaged in 164 Pins, CQFP
- SCL's 180nm CMOS Technology



Digital Baseband ASIC for NavIC User Receiver (11 Channels)



PRODUCT DESCRIPTION:

The SC1121-0 is a compact 11-channel configurable digital baseband ASIC for Navigation Indian Constellation, NavIC, SPS/RS-SHORT, GPS & GAGAN User Receivers. Designed in 180nm (TS18SL) CMOS technology, the ASIC contains Acquisition and tracking modules along with interfaces like UART. The device can operate over a large temperature range -55°C to +125°C and it is packaged in a hermetic sealed 144 pin ceramic quad flat package. The receiver capable of receiving signals at L1, L5 and S band frequencies, down-convert them to baseband, and then process them to calculate the Position, Velocity and Time solution.

FEATURES:

- 3.3V I/O power supply and 1.8 V for core
- Processor Clock 70 MHz
- ADC Sampling clock-SPS 16.368 MHz
- Power dissipation < 800 mW
- Operating Temperature: -55°C to 125°C
- Hermetic sealed 144-pin CQFP
- Capable of receiving signals at L1, L5 and S band frequencies
- 11 IRNSS Channels
- Time to First Fix (TTFF): Cold Start < 120 sec
- Acquisition Sensitivity :36 dB-Hz
- Tracking Sensitivity: 28 dB-Hz
- Navigation data rate on all signals is 25 bps
- User interface: NMEA
- ESD Sensitivity Level 2 KV HBM



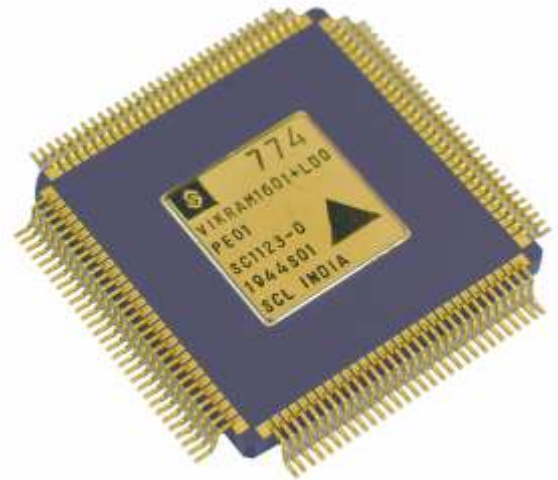
16-Bit Processor VIKRAM-1601 (PE01)

PRODUCT DESCRIPTION:

Vikram 1601 is a 16-bit microprocessor with floating point support. It has a general-purpose architecture with an instruction set of 96 instructions and employs micro programmed control. It has sixteen 16-bit registers and can address a maximum of 232K words of memory. It also incorporates a programmable counter for Real time counter function and an interface to MIL-1553B protocol controllers.

FEATURES:

- 16-Bit Microprocessor
- Single 3.3 V Supply Operation
- 75 MHz Operating Frequency
- Quiescent Supply Current < 10 mA
- Operating Power < 250 mW
- Operating Temperature -55°C to 125°C
- 120 Ceramic Quad Flat Package
- 16,32 and 48-Bit data types
- 96 Instructions
- 32-Bit single precision
- 48-Bit extended precision
- On-chip programmable counter
- On-chip 1553B bus interface
- Programmable Memory wait cycles
- SCL's 180nm CMOS Technology
- Qualified as per MIL STD 883



Vikram 1601 Processor has flown in the, guidance & control package as well as in Navigation Interface Module (NIM) with flawless performance. The Development of Vikram Processor is a significant Achievement towards in Indigenization of Key Processor used on-Board in Launch Vehicles.



32-Bit PROCESSOR VIKRAM 3201 with LVR (MCM1)



PRODUCT DESCRIPTION:

Vikram 3201 is a 32-bit microprocessor with floating point support. It has a general-purpose architecture with an instruction set of 152 instructions and employs micro programmed control. It has thirty-two 32-bit registers and can address a maximum of 4096M words of memory. The device can operate over a large temperature range -55°C to +125°C and it is packaged in a hermetic sealed 181 pin grid array package. Data type Supported are 16/32-bit Fixed Point, 16/32-bit Unsigned and 64-bit IEE754 Floating Point.

FEATURES:

- 32-Bit Microprocessor
- Single 3.3V Supply Operation
- 100 MHz Operating Frequency
- Quiescent Supply Current < 10 mA
- Operating Power < 500 mW
- Operating Temperature -55°C to 125°C
- Testability Features: Scan and Functional
- Packaged in 181 Pins, CPGA
- No of Instruction: 152
- External Address bus size: 20 bit
- Software Interrupts: 256
- No. of Timers: 4 Nos. of 32-bit timers
- Two on-chip 1553B bus interfaces
- SCL's 180nm CMOS Technology

Vikram 3201 is planned to be used in Reusable Launch Vehicle (RLV).



32-Bit PROCESSOR KALPANA 3201 with LVR (MCM3)

PRODUCT DESCRIPTION:

Kalpana 3201 is a 32-bit microprocessor with floating point support. Its architecture is based on IEEE-1754 ISA instruction set architecture. The processor employs RISC hardware control and it has floating point support. The device can operate over a large temperature range -55°C to +125°C and it is packaged in a hermetic sealed 181 pin grid array package. Data type Supported are 8/16/32/64-bit Fixed Point, 8/16/32/64-bit Unsigned and 32/64-bit IEEE754 Floating Point.



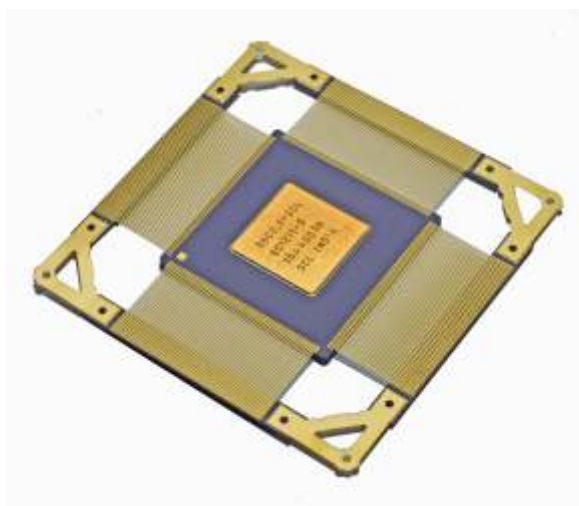
FEATURES:

- 32-Bit Microprocessor
- Single 3.3V Supply Operation
- 210 MHz Operating Frequency
- Quiescent Supply Current < 10 mA
- Operating Power < 500mW
- Operating Temperature -55°C to 125°C
- Testability Features: Scan and Functional
- No of Instruction: 107, 32 bit wide
- External Addressing bus size: 22 bit
- Interrupts: 11 (4 external, 7 internal)
- Traps: 19 exceptions
- No. of Timers: 4 Nos. of 32-bit timers
- Two on-chip 1553B bus interfaces
- Packaged in 181 Pins, CPGA
- SCL's 180nm CMOS Technology

It is planned to be used in NavIC Aided Inertial Navigation System (NAINS)



On-Board Controller ASIC (OBC- V2.1)



PRODUCT DESCRIPTION:

OBC-2.1 ASIC Architecture is based on 8-bit embedded micro-controller soft core (DW8051). The 8051 is interfaced with peripheral modules through Special Function Register (SFR) or Memory Bus. The ASIC has Mil-Std-1553 Remote Terminal (RT) functionality implement on-chip memory mapped to DW8051.

FEATURES:

- 8-bit embedded micro-controller soft core
- Single 3.3 V Supply Operation
- 48 MHz Operating Frequency
- Quiescent Supply Current < 10 mA
- Operating Power < 2 W
- Operating Temperature: -55°C to 125°C
- 256 pin Ceramic Quad Flat Package/Cerquad
- 32-bit Floating Point Coprocessor (IEEE 754 compatible)
- Total 6 UARTs (1-RS422, 3-CMOS, 2-RS485)
- On-chip SRAM: 256 x 8 bits
- ADC (Delta Sigma ADC with 8 channel MUX)
- On-chip Mil 1553B RT core
- SCL's 180nm CMOS Technology

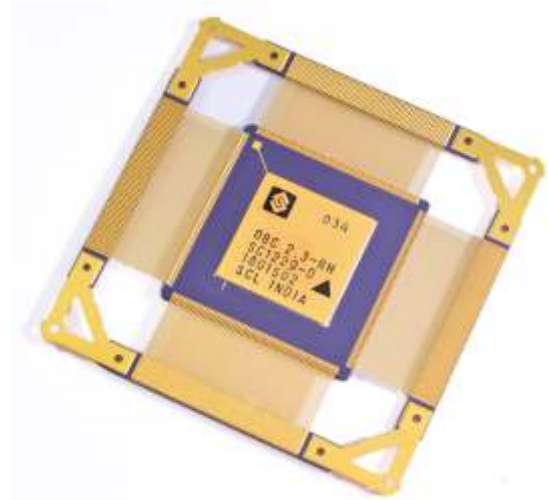


On-Board Controller ASIC (OBC- V2.3)

PRODUCT DESCRIPTION:

OBC-2.3 ASIC Architecture is based on 8-bit embedded micro-controller soft core (DW8051). The 8051 is interfaced with peripheral modules through Special Function Register (SFR) or Memory Bus.

ASIC has 32-bit Floating Point Coprocessor (IEEE 754 compatible) and total 6 UARTs (1-RS422, 3-CMOS, 2-RS485)



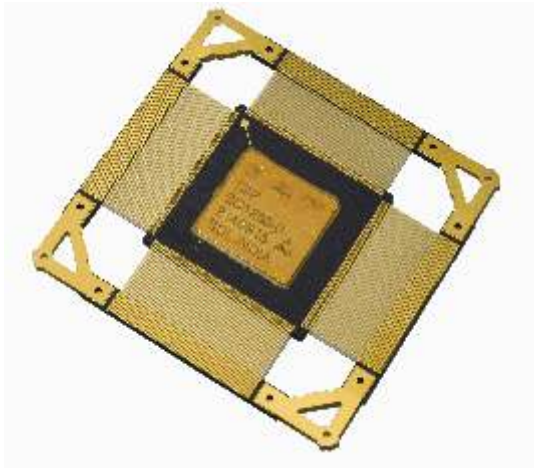
FEATURES:

- 8-bit embedded micro-controller soft core
- Single 3.3 V Supply Operation
- 24 MHz Operating Frequency
- Quiescent Supply Current < 10 mA
- Operating Power < 1 W
- Operating Temperature -55°C to 125°C
- 256 pin Ceramic Quad Flat Package
- On-chip SRAM: 1024 x 8 bits
- ADC (Delta Sigma ADC with 8 channel MUX)
- SCL's 180nm CMOS Technology
- Qualified as per MIL STD 883

The device replaces the imported devices earlier fabricated at the overseas facility. This device is successfully flown in RISAT-1A payload of EOS-04



TILE SERIAL PROTOCOL (TSP) ASIC



PRODUCT DESCRIPTION:

Tile Serial Protocol (TSP) is a custom protocol used for distributed control sub-systems of phased array radar. This protocol will be useful for communication of tele-command/telemetry data as well as communication of timing signals from central Payload Controller (PLC) to distributed T/R Controllers (TRC). The advantage of proposed protocol is huge reduction in tile harness, ease of debug and standardization of tile control management. TSP ASIC is a mixed signal ASIC consist of Digital Modules:

- Sync Pulse Generator
- Timing Signal Sampler
- Timing Signal Generator
- Frame Encoder and Decoder
- One Frame Timer
- Fail Safe Module
- Wave Encoder & Decoder
- Received Channel Selector
- Special Function Register Module
- Interrupt Generation Module
- Clock Divide Module
- Memory Wrapper
- DPRAM

Analog Modules:

Two RS-485 Differential Transceiver
LDO



Bus Extender Module ASIC (BEXM)

PRODUCT DESCRIPTION:

BEXM-RPTR is used to extend the length of the 1553B bus by means of regenerating the signal using Decoder-Encoder controller circuitry implemented.

FEATURES:

- Power Supply Core:1.8V, I/O:3.3V
- Clock Frequency 12 MHz
- Number of I/Os 16
- Types of I/Os 3.3V CMOS
- Power Dissipation 10 mW at 12 MHz
- Operating Temperature -55°C to 125°C
- Power Consumption 800 mW (max)
- Testability: Scan & Functional
- ESD Sensitivity 2KV HBM
- 64 pins Ceramic Quad Flat Package
- SCL's 180nm CMOS Technology
- Qualified as per MIL STD 883





DIGITAL SERVO LOOP (DSL) ASIC



PRODUCT DESCRIPTION:

Digital Servo loop SC1119-0 is planned to be used in ASIC based Ceramic Servo Accelerometer (CSA). High resolution acceleration output will be directly available from the sensor, dispensing with the need of digital converter circuits. The circuit blocks that are supported by 180nm CMOS technology are realized as one ASIC chip through SCL. The DSL ASIC along with differential pre amplifier and a few tuning elements will form the complete electronics for the ASIC based CSA. This will enable integration of the electronics along with the sensing within the CSA sensor housing itself

FEATURES:

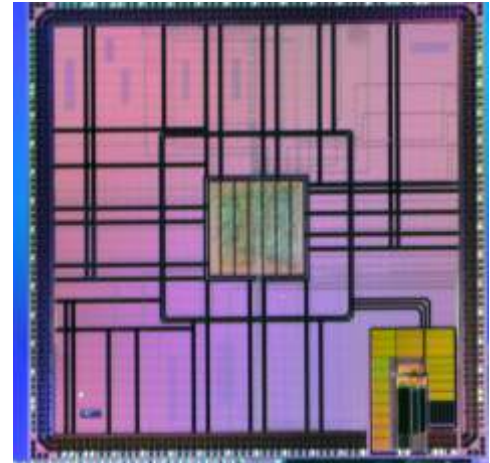
- 5V \pm 10% Single Power supply
- 30 mA Source/Sink Capability
- Low quiescent current 1uA
- $I_{IH} < 100$ nA, $I_{IL} = 250-350$ uA
- Operating Temperature -55°C to 125°C
- Packaged in 64 lead CQFP (z-type)
- SCL's 180nm CMOS Technology
- Die / Custom Package Options



MESSAGE CHECKSUM (HASH) GENERATOR

PRODUCT DESCRIPTION:

Hash Generator is a message checksum generator and a peripheral chip having a standard interface, for use with general purpose processors. It has a 16-bit bidirectional data bus (Dbus [15:0]), address lines [3:0], control signals (CS_, WR_RD_, and RST_), configuration signal nm, 13 clocks and 2 output signals. The message checksum generator block generates message checksum in two modes of operation i.e. MODE-0 and MODE-1. It is implemented as digital logic. In mode0, data from a self-sustaining source is sampled periodically and post-processed for generating the message checksum. This is the free-running mode. In mode-1 a known input is applied, by the processor. Each block of data is written into message checksum generator block and further processed by the post-processing block to produce the checksum.

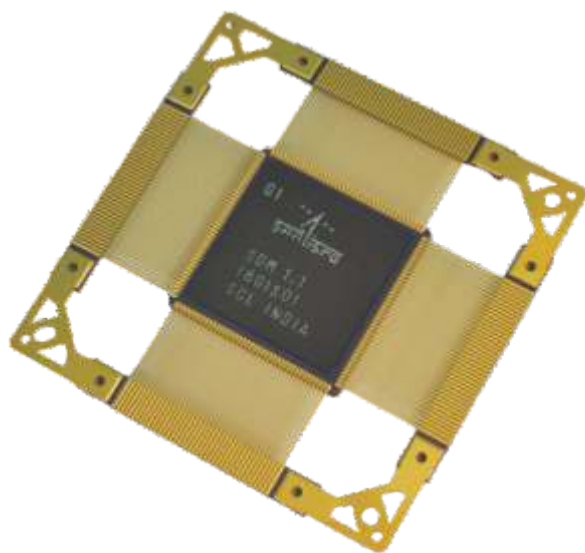


FEATURES:

- SC1219-0 (Power Supply: 5V±0.5V)
- SC1137-0 (Power Supply: 3.3V±0.3V)
- 4 mA Source/Sink Capability
- Supply Current: 3mA
- Operating Temperature: -55°C to 125°C
- SCL's 180nm CMOS Technology
- Die / Custom Package Options



MODEM IN-DOOR UNIT (MIDU) ASIC



PRODUCT DESCRIPTION:

MIDU ASIC has been developed to form a crucial component in any of the ground based SATCOM Terminal. It supports wide range of Modulation schemes (BPSK/QPSK/8-PSK/16-QAM), Forward Error Correction techniques (Convolution, Reed-Solomon & Turbo). MIDU caters Data rate ranging from 2.4 Kbps to 40 Mbps & IF from 0 to 25 MHz. MIDU supports 3 modes for configuration and M&C i.e. SPI, UART & JTAG.

FEATURES:

- 3.3 V I/O pads Power Supply
- 1.8 V Core Supply
- SCL's 180nm CMOS Technology
- Operation clock frequency 100 MHz
- 107 I/O's with 3.3V LVTTTL
- Interface: SPI, UART, JTAG
- Operating Temperature -40°C to 85°C (Industrial grade)
- Testability Features: Scan and Functional
- Packaged in 164 Pins CQFP



SEMICONDUCTOR MEMORIES



2M bit Synchronous SRAM



PRODUCT DESCRIPTION:

SC1702-0 is 2 MBit Synchronous SRAM designed in SCL's 180 nm CMOS technology. 128Kbit of a memory is replicated sixteen (16) times to get the 2Mbit of memory. The arrangement is of Four (04) numbers of rows and four (04) numbers of columns of the 128 Kbit memories. Memory has 17 address lines (A0 to A16) and 16 data lines (DIO_0 to DIO_15). A Chip Select (CSB) pin allows the user to deselect the device when desired. If CSB is high, no new memory operation is initiated. OEB enables read and WEB enables write operations at rising edge of CLK. No operations will be performed on falling edge of CLK.

FEATURES:

- 3.3V Power Supply for I/O pads
- 1.8 V Supply for Core
- High speed 40 MHz operation
- Access Time 10ns
- Operating Temperature -55°C to 125°C
- SCL's 180nm CMOS process technology
- Packaged in 68 lead CQFJ



256K Bit, 32K X 8 ASYNCHRONOUS SRAM

PRODUCT DESCRIPTION:

The SCL SC1301-1 is a high performance CMOS static RAM organized as 32,768 words by 8 bits. Writing to the device is accomplished by taking Chip Select (CS) and Write Enable (WE) inputs LOW. Reading from the device is accomplished by taking Chip Select (CS) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. The input/output pins (I/O1 through I/O8) are placed in a high-impedance state when the device is deselected (CS HIGH), or OE and WE both are held HIGH with CS Low. The SCL SC1301-1 is available in standard 68-pin CQFP SOJ packages.



FEATURES:

- 3.3V Power Supply for I/O pads
- 1.8 V Supply for Core
- High speed 25 MHz operation
- Access Time 22 ns
- Operating Temperature -55°C to 125°C
- SCL's 180nm CMOS process technology
- Packaged in 68 lead CQFP-J



RADHARD DUAL PORT SRAM 4K x 8



PRODUCT DESCRIPTION:

Triple modular Redundancy (TMR) technique using voting logic is used to realize Radhard Dual Port SRAM. Additional logic cells used in realizing TMR along with buffering had been selected from SCL's RH standard cell library. In dual port memory, each port (labelled 1 or 2) is completely independent, and there are no constraints on the timing of the ports relative to each other except in the case of address contention. Because ports 1 and 2 are completely symmetrical, the descriptions apply to both ports: to differentiate the ports, the term PIN_p is used to reference PIN of port "p" where p is either 1 or 2.

FEATURES:

- 3.3V Power Supply for I/O pads
- 1.8 V Supply for Core
- Synchronous Operation (50MHz)
- Operating Temperature -55°C to 125°C
- Packaged in 64 pin Cerquad
- SCL's 180nm CMOS process technology
- TID immune upto 100 kRad.
- SEU/SEL immune up to 70 MeV-cm²/mg
- chip size 2.350 x 2.000 mm²



IMAGERS & DETECTORS



FRAME TRANSFER CCD IMAGER 4K X 48



PRODUCT DESCRIPTION:

The SD 3101 is a frame transfer area CCD Image Sensor with 48 rows of 4000 pixels each, designed to be operated in off-chip TDI Mode. The parallel and serial readout registers are 4 - phase, N-buried Channel Type. To reduce on chip power dissipation- Output port cascading feature is provided for operation at low rate with reduced number of output.

FEATURES:

- 10 μm square pixels with 10 μm pitch.
- 4000 x 48 Frame Transfer Architecture.
- 8 output ports with cascading features.
- Wave length range 410 nm to 1010 nm.
- 64 pin ceramic DIP package.



FRAME TRANSFER CCD IMAGER 1K X 60

PRODUCT DESCRIPTION:

SD3113-0 device is a Frame transfer CCD. The Image Region consists of an array of 1000 x 60 for sensing of the image and collection of the photo-generated charge. Image region is split in two parts, which is subsequently readout through four Readout Shift Registers; two shift register is at top of the image region and other two shift register is at bottom of the image region. Image region and storage is separated by 8 dark isolation rows and 3 unshielded rows. Each readout shift register is terminated in an Output Section. The electrical points in the device are accessed through Device Pads.



FEATURES:

- Array Size: 1000 x 60
- Pixel Pitch: 11 μm
- Pixel Size: 11 μm x 26 μm
- Conversion Gain: $\sim 4 \mu\text{V}/\text{e}$
- Dark Isolation Rows: 8 (B/w Image and storage region)
- Dark Isolation Columns: 6 (Both sides)
- Output Ports: 4
- Vertical Transfer: 4 phase
- Horizontal register Transfer: 4 phase
- SCL 0.18 μ CMOS technology



12K VISIBLE CCD TDI IMAGER



PRODUCT DESCRIPTION:

The SD3301 is a high resolution, high data rate, 12288 pixels visible TDI linear imager. Each pixel consists of 96 stages of CCD (photo-gate) sensors for charge integration. There are twenty-four readout shift registers for high data rate. The parallel shift registers are of 4-phase N-buried channel type, serving the multiple purposes of photo-detection, charge integration and charge transfer. For a particular rate of transfer in the parallel shift register, the integration can be varied using 2, 8 or 32 stages instead of all the 96. This is done by applying appropriate clock signals to the corresponding pins.

FEATURES:

- Pixel Size: $8\text{ }\mu\text{m} \times 8\text{ }\mu\text{m}$
- Pixel Pitch: $8\text{ }\mu\text{m}$
- Maximum integration stages: 96
- Variable number of integration stages
- Twenty-four outputs for fast readout
- Cascading feature for reduced number of outputs.



Advanced Linear Imaging Scanning Sensor 14032 X 1

PRODUCT DESCRIPTION:

ALISS or Advanced Linear Imaging Scanning Sensor is a single array photodiode CCD sensor. It consists of linear 14k photo-diodes and 16 isolation pixels on both left and right side of the photodiode array. Each pixel has two storage gates and a transfer gate connecting the horizontal shift registers (HSR). The architecture has 10 sets of HSRs i.e., 1400 pixels per HSR set. Odd pixels are readout through port 1 to port 5 and even pixel are readout through port 6 to port 10. Two variants have been fabricated, SD3002-0 with anti-blooming and SD3005-0 without anti-blooming.

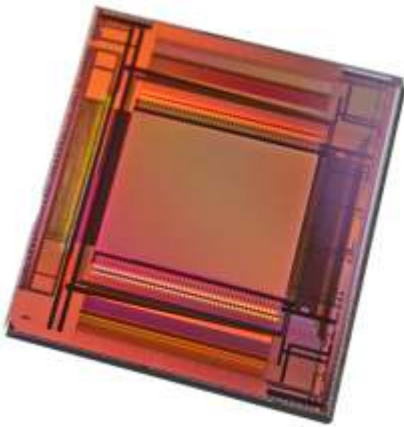


FEATURES:

- Device size: 116.1 mm X 5.2 mm
- Active elements: 14032 X 1 pixels
- Pixel Pitch: 8 μm
- Video Outputs: 10
- Elements per readout: 1400
- Vertical Transfer 2-phase
- Vertical Line Transfer Rate: 0.33 kHz
- Horizontal register transfer: 4-phase
- Readout Rate: 0.5 MHz
- Anti-blooming feature available in one variant.



ROIC



PRODUCT DESCRIPTION:

The ROIC developed at SCL is of active array size 384 x 288 with 2 dummy rings around active array. This ROIC is a slave mode device which needs master clock, master reset, frame sync and Integration signal as inputs and gives out Line sync signal, Data Synchronization signal to user along with two analog outputs. It supports two readout modes and works in snapshot mode only. User can choose various operating modes by programming control register using serial interface and can even use the default mode of operation. Programming of control register can be done by writing the appropriate control word into the control register with the help of SPI.

FEATURES:

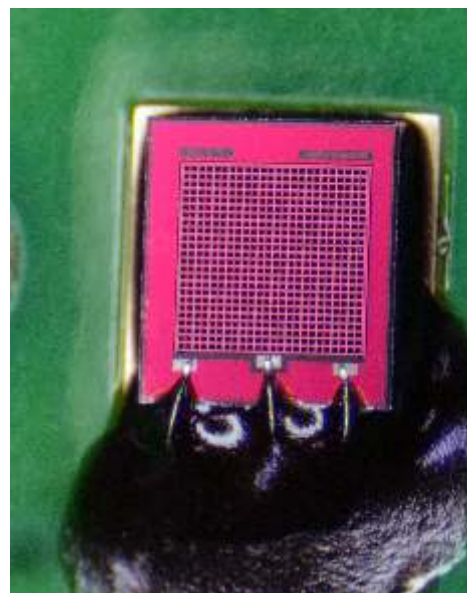
- Basic Array Size: 384 x 288
- Array Size (Dark Rings): 388 x 292
- Pixel Pitch: 15 μm
- Indium Bump Opening: 7 μm
- Output Ports: 2
- Output Rate: 20 MHz (Analog)
- Frame rate (Max): 140 fps
- Output Range (Min): 1 V
- Readout mode: ITR/IWR
- Temperature Sensors: 4
- Programmable Well Capacitance: 3 & 2 Me
- Total Average Power: 94 mW
- H-flip and V-flip: Yes
- Operating Temperature (TA): 77K to 100K
- SCL 0.18 μ CMOS technology



SILICON PHOTOMULTIPLIER

PRODUCT DESCRIPTION:

Silicon Photomultiplier is a novel, high gain, single photon sensitive sensor. It consists of parallel array of identical and independent avalanche photodiodes pixels, with each pixel diode connected to bias voltage supply through a series resistor (~few hundred kilo Ohms). Device are available in: 1.5 x 1.5 sq. mm (pixel size 50um x 50um & 10um x 10um) 3 x 3 sq. mm (pixel size 50um x 50um & 10um x 10um) 3mm circular diameter

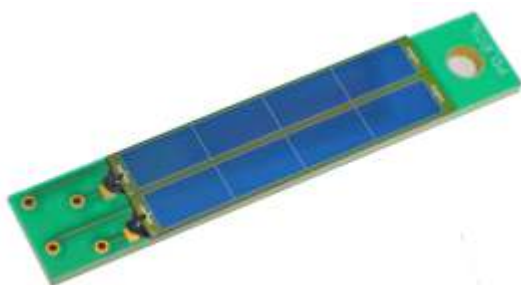
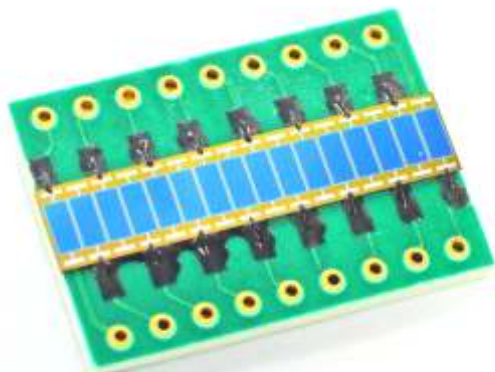


FEATURES:

- Breakdown Voltage (BV): 22 V
- Over-Bias voltage: 2V (max)
- Temperature coefficient of BV: 22mV/°C (Temperature Range :-243to 323 K)
- Total leakage current :<5nA/cm² (at 20 V)
- Dark count rate: 350 to 700kHz (3*3 sq mm) & 370 to 500 kHz (1.5*1.5 sq mm)
- Recovery time: 100ns
- Geometrical Fill factor: 70% for 50 um pixel size & 15% for 10 um pixel size SiPMs



Photodiode Detectors for X-Ray Systems



PRODUCT DESCRIPTION:

X-Ray Baggage (Type-A) and Cargo Inspection Systems (Type-B) for scanning of objects for security purpose. The systems currently use imported diode array detectors. SCL has taken up the fabrication of PIN photodiode arrays for these applications. The photodiodes are large area P-I-N photodiodes fabricated on high resistivity n-type float zone wafers. The diodes are enclosed in P+ guard ring.

FEATURES:

- No of pixels: 16 (Type-A)/ Single Photodiode (Type-B)
- Pixel size: 3.2mm × 1.4mm/ 3cm × 0.4cm
- Pixel pitch: 1.5 mm
- Chip size: Approx 3.2mm × 24mm / Approx 3.5cm × 0.5cm
- Dark current < 500pA @ 10V/ < 1nA @10V
- Responsivity - 0.3 A/W at wavelength of 540nm



SENSORS



Uncompensated Pressure Sensors



PRODUCT DESCRIPTION:

SCL's MEMS based pressure sensors are in the form of Bridge of four piezo-resistors to give differential output proportional to applied pressure. The absolute sensors have an internal vacuum reference. These are intended for use with Non-corrosive, Non-ionic working fluids; such as air and dry gases.

FEATURES:

- Operating Ranges : Upto 30 bar
- Package : TO headers / PCB (COB)
- Custom Package option available
- Sensor dies are available



Uncompensated Oil Filled Pressure Sensors

PRODUCT DESCRIPTION:

SCL is involved in developing MEMS based Pressure sensors. Sensors are in the form of Bridge of four peizo-resistors to give differential output proportional to applied pressure. The absolute devices have an internal vacuum reference.

Pressure sensor silicon die, encapsulated in SS316L housing filled with oil, is intended for harsh & corrosive environment and media isolation.



FEATURES:

- Operating Ranges : 1 to 30 Bar
- Measurement Mode : Absolute
- Bridge Resistance : 2.0K to 4.0K
- NL+H <0.2%
- Package : TO Header
- Housing & Diaphragm : Stainless Steel AISI 316 L



Temperature Compensated Analog Output Pressure Sensors



PRODUCT DESCRIPTION:

SCL developed MEMS based Pressure sensors are in the form of Bridge of four peizo-resistors to give differential output proportional to applied pressure. Absolute pressure sensor has an internal vacuum reference. Pressure Transducer is fully calibrated and temperature compensated for sensor offset, sensitivity, temperature effects using an on-board application specific integrated circuit (ASIC). Calibrated output values for pressure are updated at approximately 1 kHz.

Transducer comes with pre programmed calibration coefficients, loaded into EEPROM. Transducer provides corrected output voltage.

FEATURES:

- Operating Voltage $5V \pm 0.5V$
- Ratiometric/Non Ratiometric Output
- Absolute Pressure Range upto 10 Bar
- Operating Temperature: $-20^{\circ}C$ to $85^{\circ}C$
- Tight accuracy of 0.25% of FSS (BFSL)
- Total Error Band (TEB) $< 0.5\%$ FSS
- Enhanced sensor interchange ability
- PCB mountable 8-Pin DIP Package
- Intended for measuring pressure of Non-corrosive, Non-ionic working fluids; such as air and dry gases.
- Customized Package Options based on application requirement



Temperature Compensated Digital Output (I2C/SPI) Pressure Sensors

PRODUCT DESCRIPTION:

SCL developed MEMS based pressure sensors are in the form of Bridge of four peizo-resistors to give differential output proportional to applied pressure. Absolute pressure sensor has an internal vacuum reference. Pressure sensor module is fully calibrated and temperature compensated for sensor offset, sensitivity and temperature effects. Sensor comes with pre programmed calibration coefficients, loaded into EEPROM. Sensor provides 16-bits corrected pressure data over I2C bus. Pressure sensor die along with signal conditioner IC are assembled in a single 7-pin TO package.

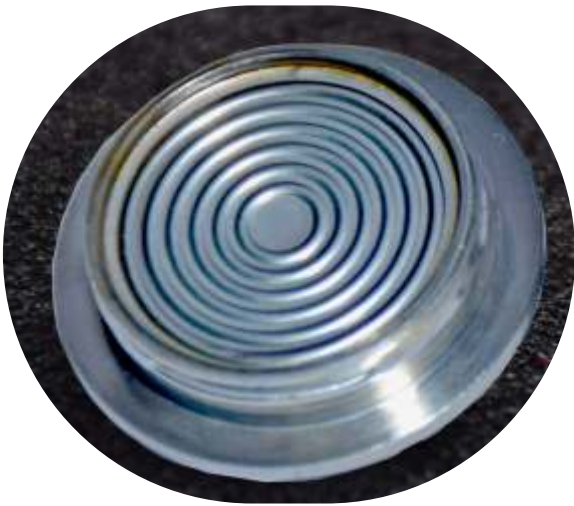
FEATURES:

- Operating Voltage 1.8V to 3.6V
- 16-Bit I2C/SPI Output
- Operating Temperature: -40°C to 110°C
- Pressure Range upto 30 Bar
- Total Error Band less than 0.25% FSS
- Fully Corrected Signal at digital output
- Suitable for Non-corrosive, Non-ionic working fluids; such as air and dry gases.





Temperature Compensated Digital Output (I2C/SPI) Oil Filled Pressure Sensors



PRODUCT DESCRIPTION:

SCL developed MEMS based pressure sensors are in the form of Bridge of four piezo-resistors to give differential output proportional to applied pressure. Absolute pressure sensor has an internal vacuum reference. Pressure sensor module is fully calibrated and temperature compensated for sensor offset, sensitivity and temperature effects. Sensor comes with pre programmed calibration coefficients, loaded into EEPROM. Sensor provides 16-bits corrected pressure data over I2C bus.

Sensor die along with signal conditioner, encapsulated in SS316L housing filled with silicone oil, is intended for harsh & corrosive environment and media isolation.

FEATURES:

- Operating Voltage 1.8V to 3.6V
- 16-Bit I2C/SPI Output
- Operating Temperature: -40°C to 110°C
- Pressure Range upto 30 Bar
- Total Error Band less than 0.25% FSS
- Fully Corrected Signal at digital output
- Package : 7-pin TO Header
- Housing & Diaphragm : Stainless Steel AISI 316 L
- Suitable for harsh & corrosive environment and media isolation.



Radiation Hardened Digital Output (SPI) Pressure Sensor

PRODUCT DESCRIPTION:

SCL developed MEMS based Pressure sensors are in the form of Bridge of four peizo-resistors to give differential output proportional to applied pressure. Absolute pressure sensor has an internal vacuum reference. Pressure Sensor is calibrated and temperature compensated for sensor offset, sensitivity, temperature effects using in-house developed 24-bit sensor signal conditioner IC. In-house developed PRT is used for temperature compensation. Each transducer is temperature compensated & calibrated. Transducer comes with calibration coefficients. SPI master, usually a microcontroller, will read 24-bit pressure and temperature data and apply provided calibration coefficients to get corrected pressure data.



FEATURES:

- Operating Voltage $3.3V \pm 0.3V$
- 24-Bit SPI Output
- Pressure Range 2.2, 5.0 Bar
- Operating Temperature: $-40^{\circ}C$ to $85^{\circ}C$
- Radiation hardened upto TID levels of 100 kRad
- Immune to SEL, SET upto 50 MeV-cm²/mg
- PCB mountable 8-Pin DIP Package



Digital Output (SPI) Accelerometers

PRODUCT DESCRIPTION:

MEMS based Capacitive Accelerometer measures acceleration along a single axis. MEMS die changes its capacitance when acceleration is applied. Signal conditioner IC converts change in capacitance into 24-bit digital output. Digital output is provided in the range of 800000 to 7FFFFFFF for –FSR to +FSR. Both MEMS die and CMOS signal conditioner IC are hermetically packaged in a single 44 pin MCM CLCC package. Option of uncommitted Pt based temperature sensor (PRT) within same package. Each sensor is calibrated. Sensor comes with calibration coefficients.

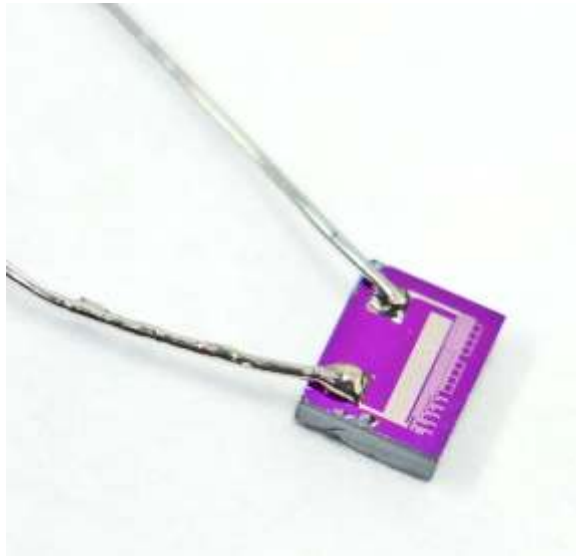


FEATURES:

- Full Scale Ranges : 2g, 5g, 10g, 30g, 50g
- Supply Voltage: 3.0V to 3.6V.
- 24-Bit Signed Digital Output
- SPI Compatible Serial Interface
- On Chip CMOS Temperature Sensor
- Offset & Gain Calibration
- Temperature Range : -40°C to 125°C
- Transducer Package : 44-Pin CLCC
- Custom Package Option Available
- Package Size : 16 mm x 16 mm x 2.8 mm



Temperature Sensor (PRT)



PRODUCT DESCRIPTION:

Temperature sensors are thin film platinum based PRTs. Nominal resistance at ambient is around 1 K Ω with sensitivity of 3 Ω /°C.

Sensor variants with nominal resistance R0 values of 100 Ω , 500 Ω & 1500 Ω can also be customized as per application requirements.

FEATURES:

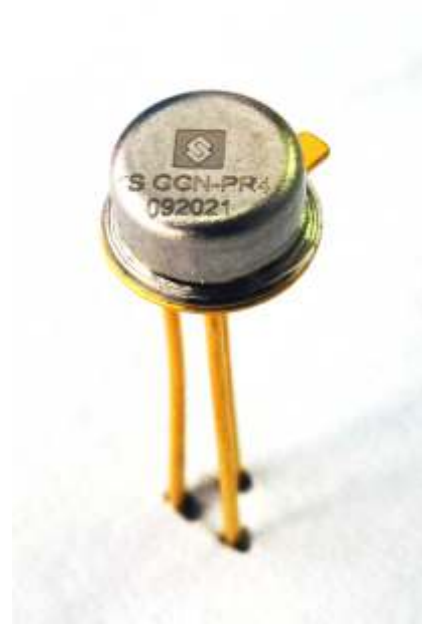
- Operating Ranges : -20°C to 100°C
- Accuracy : 1°C
- Nominal Resistance (25°C) : 1K Ω \pm 5%
- Sensitivity : 3 Ω /°C
- Package : TO-46/52, Bare Dies, Custom
- Die Size : 2.0 mm x 2.5 mm x 0.675 mm



Band Gap based Temperature Sensor SC1025-0

PRODUCT DESCRIPTION:

The device is low voltage, precision centigrade temperature sensor which provides output voltage directly proportional to Celsius temperature. The core circuit comprises of traditional CTAT and PTAT block. Both CTAT and PTAT are BJT based blocks to improve performance. Cascode structures are used to improve mirroring and PSRR. The CTAT is subtracted from PTAT to obtain desired output and sensitivity. The output of core block is: $\text{Output} = \alpha * \text{PTAT} - \beta * \text{CTAT}$ Where α and β are scaling factor used to scale the output voltage and sensitivity.



FEATURES:

- Power Supply Range: $3V \pm 0.3V$
- Supply Current: 300 μA
- Temperature range $-20^{\circ}C$ to $120^{\circ}C$
- Non-Linearity: $0.25^{\circ}C$ (BFSL, $25^{\circ}C$ to $100^{\circ}C$)
- Error: $0.2^{\circ}C$ (2nd-Order, $-20^{\circ}C$ to $120^{\circ}C$)
- Scale Factor (Typical): 11.5 mV/deg. C
- Typical Output Voltage (at $25^{\circ}C$): 675 mV
- 8 pin flat /SOP Package, TO Package Die size: 0.68 mm x 0.75 mm, Thickness :0.725mm
- Standard 180 nm CMOS Technology





Piezo-Electric Acoustic Sensor

PRODUCT DESCRIPTION:

SCL has developed AlN based piezoelectric acoustic sensors. Utilizes silicon diaphragm as main Sound Pressure to lateral stress converter and AlN as stress to electric charge converter.



FEATURES:

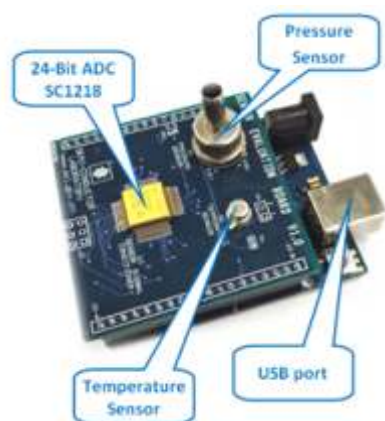
- Measurement Range, 100 -180dB
- Linearity better than 1.5dB
- Full Scale Output $\pm 2.5V$ (adjustable)
- Frequency Range 31.5Hz to 6.3kHz
- Housing & Diaphragm SS AISI 316 L



ACADEMIA BOARDS



SCL Sensor Evaluation Board SSEB V1.0 Pressure and Temperature Monitor for Lab



DESCRIPTION:

SCL Sensor Evaluation Board SSEB V2.0 is aimed to evaluate following components: .

- SCL Temperature Sensor (PRT)
- SCL Pressure Sensor (1.5 Bar)
- SCL Readout ASIC SC1218
- Other Commercial Resistive Sensors

SSEB V1.0 is aimed to help students to learn:

- Analog front-end & Sensor Signal Conditioning.
- Calibration & Temperature Compensation algorithm.
- Evaluates their own developed or commercial available sensors
- Develop & Implement their own algorithms.

FEATURES:

- EV Board provides corrected Pressure & Temperature readings in different scientific units.
- EV Board comes with programmed calibration coefficient for SCL sensors.
- Factory settings may be restored with calibration coefficient provided in KIT.



Pressure Range	Upto 1500 mBar
Accuracy	1.0% Range
Temperature Range	0°C to 50°C
Accuracy	0.5°C
Supply	+5V (from USB port)
Data Interface	USB Port



SCL Sensor Evaluation Board SSEB V2.0 Inclinometer/ Tilt Measurement



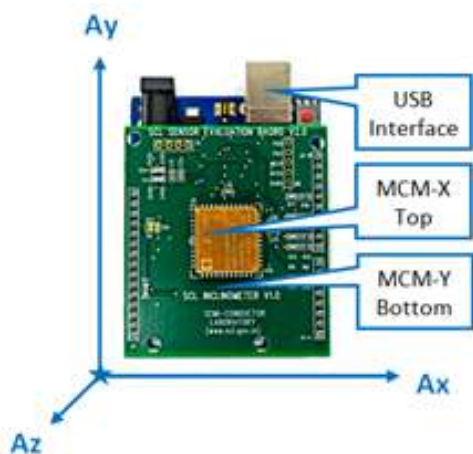
DESCRIPTION:

SCL Sensor Evaluation Board SSEB V2.0 is aimed to evaluate following components:.


- SCL Capacitive Accelerometer (1.2g)
 - Accelerometer Signal Conditioner SC1259
- SSEB V2.0 is aimed to help students to learn:
- Capacitive Sensor Signal Conditioning.
 - Calibration & Temperature Compensation algorithm.
 - Student may use this for developing g force measurement applications such as rover, drone, tilt measurement etc.

FEATURES:

- Two accelerometers Multi Chip Modules (MCMs) are used to measure inclination angles of X & Y axis.
- The tilt angle/acceleration along X & Y- axis is readout using in-house developed C sharp based GUI software.



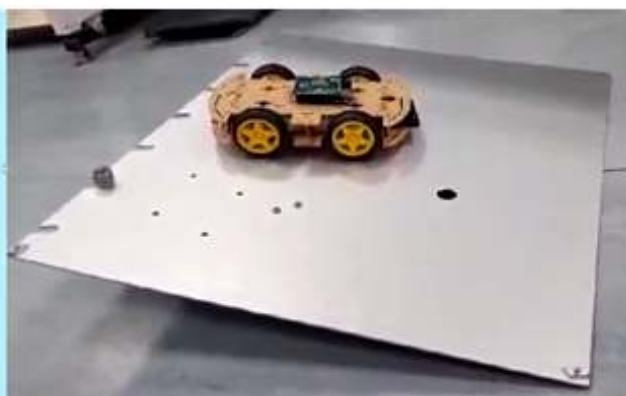
Range	± 45 degrees
Resolution	0.01 degree
Scale Factor	0.035 pF/degree
Supply	+5V (from USB port)
Data Interface	USB Port



Semi-Conductor Laboratory
Ministry of Electronics and Information Technology (MeitY)
Government of India.

SCL INCLINOMETER

	X-Axis	Y-Axis	Z-Axis
Tilt (Degrees)	3.5	7.7	8.5
Acceleration (g)	0.06	0.13	
Capacitance (pF)	0.13	0.29	





Quality Policy

SCL shall always strive to maximize customer's Satisfaction through :

- Commitment of every individual
- Technological upgradation
- Timely delivery of Quality Products
- Continual improvement



Commitments

- Design and manufacture advanced technology-based VLSI devices and MEMS systems & sub-systems to support strategic needs of the country.
- Provide services for the assembly and packaging of silicon wafers in ceramic packages and chip-on-boards.
- Facilitate testing, reliability & quality assurance, and failure analysis mechanisms for existing and prospective semiconductor-based microelectronic products.
- Undertake, aid, promote, guide, and coordinate research to promote the development of the semiconductor ecosystem in India





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